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The Logic of Bidirectional Binary Counters*

MARCEL J. E. GOLAY†

Summary—The counters without short-time internal memory, conceived by Bigelow, disclosed by Ware, and extended by Brown, are discussed from the standpoint of their respective logic. It is shown that the (self-instructed) bidirectional[1] counter of Brown has a more rigorous logic than the unidirectional counter of Ware; the operation of Brown's bidirectional counter being subjected to the only restriction that its speed be compatible with the operating speed of its individual toggles, whereas the operation of Ware's counter is predicated upon the existence of unspecified buffering states in the input of each stage, to prevent run-away conditions. These buffering states, which occur naturally in Brown's bidirectional counter, can be provided explicitly in unidirectional counters by replacing the two transfer circuits of Ware's counter stage, which are controlled only by one toggle of the preceding stage, by two of the four transfer circuits of Brown's bidirectional counter stage, all four of which are controlled by both toggles of the preceding stage.

This paper introduces the viewpoint that a bidirectional counter of Brown's type is a counter in which the state of one toggle of each stage determines which toggle of the next stage is master, while the state of the other toggle of each stage determines whether the slave of the next stage shall be like or unlike the master. This viewpoint permits a succinct discussion of the several possible interstage connections, and of the several counting codes obtained for each connection. In particular, it can be shown with a minimum of steps that the code exhibited by the "true" toggle is always binary, or a simple modification thereof, while the code shown by the "false" toggle is always the Gray code, or a simple modification thereof.

Introduction

In a first article,[2] Ware discussed the concept, based on a principle originally suggested by J. H. Bigelow, of unidirectional counters without short-time internal memory. This new type of counter employs a pair of toggles in each stage and transfer circuits, which alternately cause toggle F_i to be like toggle T_i, and toggle T_i to be unlike toggle F_i. This arrangement differs basically from the usual type of Eccles-Jordan bistable toggle stage, for the latter obeys the single command: "Change," which, if analyzed in terms of the operations required, means, "Remember for a short time what you are now, and become different from that." The requirement of a short-time memory in the single toggle counter stage derives from the first half of the order written above, whereas in Ware's counter stage the previous state of the toggle which has just changed is stored in the other toggle until the next command. Ware noted that two additional transfer circuits with separate instructions could permit a counter to operate bidirectionally. But in a subsequent article,[3] Brown noted that four internally instructed transfer circuits would permit a counter to reverse its counting direction, without separate instructions.

The purpose of this discussion is to examine the basic difference between the logic of Ware's unidirectional and Brown's bidirectional counters, and to introduce a point of view which permits a succinct representation and classification and a direct examination of the several types of internal logic which are possible with these bidirectional counters.

Discussion

The counter stage of Ware, which consists of two toggles and two causal connections (gates, transfer circuits) between these, is characterized by a curious difference between its input and its output. Its input is essentially ternary, for it may be either a "1" from the preceding T_{i-1} toggle, which commands toggle F_i to be like toggle T_i, or a "0" from the T_{i-1} toggle, which commands toggle T_i to be unlike F_i, or a "neither," which implies that "0" and "1" must not coexist during changes.[4] This third buffering condition, not explicitly provided in Ware's counter stages, is required to prevent the first two conditions from overlapping, for such an overlap would cause a "runaway" condition. Conversely, the stage output is double binary, for it consists of the two states of each toggle. Only half of this output, *i.e.*, the state of the T toggle, is utilized as input to the following stage, without explicit provision for the third buffering state, the "neither" condition mentioned.

In contrast, Brown's bidirectional counter stage is characterized by an input and an output which are both double binary; this provides automatically the buffering transition states just mentioned, as seen below.

Fig. 1 illustrates one of several possible cause and effect connections between an $(i-1)$st and an ith stage in a bidirectional counter of the type described by Brown. These connections are represented by four compartments in a plane, whose coordinates are the voltages in the X_{i-1} and Y_{i-1} toggles, which are conveniently represented by the same symbols.[5]

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[1] In this discussion, the expression "bidirectional counters" will refer exclusively to selfinstructed bidirectional counters, the expression "reversible counters" being reserved for counters requiring separate instructions for a reversal of the direction of counting.

[2] W. H. Ware, "The logical principle of a new kind of binary counter," Proc. IRE, vol. 41, pp. 1429–1437; October, 1953.

[3] R. M. Brown, "Some notes on logical binary counters," IRE Trans., vol. EC-4, pp. 67–69; June, 1955.

[4] The physical interpretation of this requirement, in the case of an electronic counter, is that the two conductors carrying the voltages of the two plates of the T_{i-1} toggle should never both carry, during a change of the T_{i-1} toggle, a voltage high enough to operate simultaneously the two respective transfer circuits they control.

[5] The X and Y symbols are used in preference to Ware's and Brown's T and F in order to maintain symmetry in the presentation, and to avoid a premature conclusion as to the respective toggle functions. These symbols are variously used to designate a toggle, or the quantized, "0" or "1," state of a toggle, or again some "analog" parameter of a toggle such as voltage. Simplicity without ambiguity has resulted from this multiple use of the same symbols.

The four compartments shown in Fig. 1 are nearly quadrant shaped, as "and" gates[6] would make them, and within each, one of the following four conditions exists: if $X_{i-1}=1$ and $Y_{i-1}=1$, then $Y_i \rightarrow X_i$ (X_i is made like Y_i); if $X_{i-1}=0$ and $Y_{i-1}=1$, then $\overline{Y}_i \rightarrow X_i$ (X_i is made unlike Y_i), etc. Instead of inactive buffer zones, an overlap of active zones has been illustrated, in order to emphasize the immunity of this system to zone overlap as long as the state of the input is represented by a point which travels from quadrant to adjacent quadrant by crossing two lines only in the $X_{i-1}Y_{i-1}$ plane. For instance, the overlap of the $Y_i \rightarrow X_i$ and $\overline{Y}_i \rightarrow X_i$ zones means that during a transition, the slave X_i toggle is temporarily subjected to conflicting requirements, but, since the master Y_i toggle remains unaffected, the situation is resolved unambiguously at the end of the transition. Likewise, the overlap of the $X_i \rightarrow Y_i$ and $Y_i \rightarrow X_i$ zones means that during a transition, both toggles are master and slave simultaneously, but to the same end, namely likeness of their states, so that no action can take place during this transition.

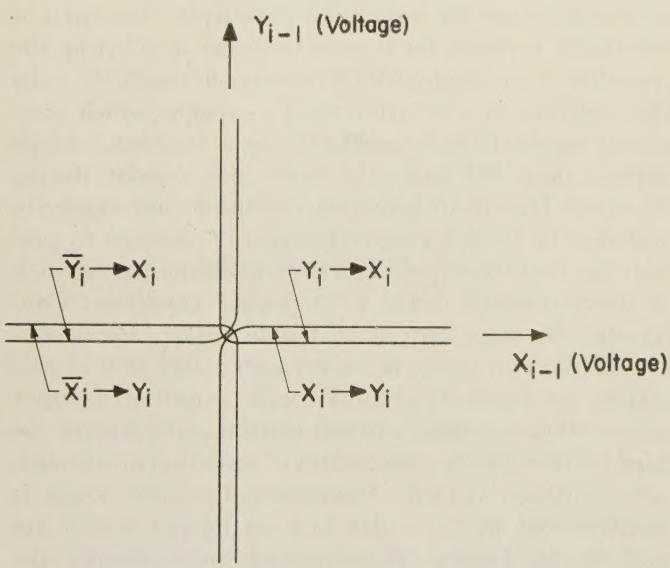

Fig. 1—Cause and effect from $(i-1)$st to ith stage by means of "and" gates.

The immunity of the system to zone overlap permits replacing the "and" gates by simple gates, each controlled by the addition of two voltages. For instance, the "and" gates which perform the logical function.

$$\text{when } X_{i-1} = 1 \text{ and } Y_{i-1} = 1$$
$$\text{then } Y_i \rightarrow X_i$$

can be replaced by a simple gate which performs the logical functions

$$\text{when } X_{i-1} + Y_{i-1} > A$$
$$\text{then } Y_i \rightarrow X_i$$

where X_{i-1} and Y_{i-1} in the inequality designate the voltages of the $(i-1)$st stage toggles, and where A is so chosen that the gate is opened when these voltages are both high, and only then.

The straight line $X_{i-1}+Y_{i-1}=A$ determines the half plane to the right of and above it, in which the transfer $Y_i \rightarrow X_i$ is activated, and has been illustrated in Fig. 2, together with the other three lines along which the three voltages $X_{i-1}-Y_{i-1}$, $-X_{i-1}-Y_{i-1}$, and $-X_{i-1}+Y_{i-1}$ determine similar boundary conditions for the respective operation of the other three gates: $\overline{Y}_i \rightarrow X_i$, $\overline{X}_i \rightarrow Y_i$, and $X_i \rightarrow Y_i$.

When Figs. 1 and 2 are compared, it is noted that the nearly quadrant-shaped zones of Fig. 1 are replaced by half-planes in Fig. 2, in which there are now four quadrant zones of double causation, four strip zones of single causation, and an internal rectangular zone of no causation. Clockwise or counter-clockwise input changes can take place along the dotted rectangle shown, which may either cross or not cross the quadrants.[7]

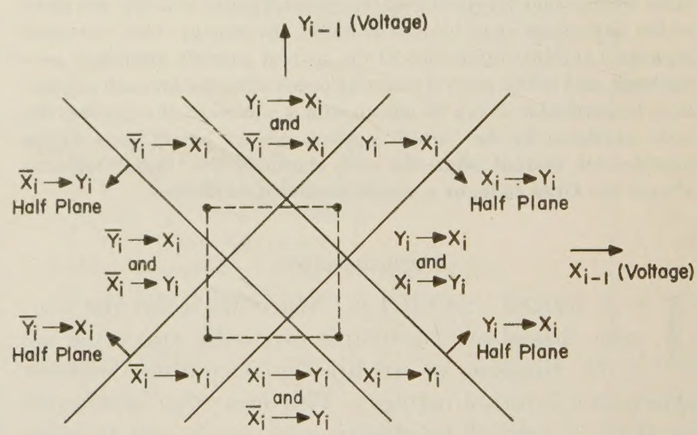

Fig. 2—Cause and effect from $(i-1)$st to ith stage by means of simple gates.

It follows from the foregoing that a unidirectional unambiguous counter can be realized by providing only the two gates corresponding to opposite strips, which are required for a given direction of rotation of the $X_{i-1}Y_{i-1}$ point (*e.g.*, the $\overline{X}_i \rightarrow Y_i$ and $Y_i \rightarrow X_i$ gates in the case of a clockwise rotation of the $X_{i-1}Y_{i-1}$ point), but that the full unambiguity of such a counter is predicated upon each operating gate being controlled by both toggles of the preceding stage, either on an "and," or on a voltage addition basis.

It can be concluded from the above discussion of the counter logic illustrated by both Figs. 1 and 2 that the causality between the $(i-1)$st and ith stages is exactly as if the Y_{i-1} state determined whether X_i or Y_i is

[6] The pair of gates required for a single transfer circuit between two toggles will be referred to simply as a gate.

[7] If the $X_{i-1}Y_{i-1}$ point travels clockwise starting at the lower right-hand corner of the rectangular path illustrated, where $X_{i-1}=1$, $Y_{i-1}=0$, and if $X_i=Y_i=0$ at the start, the X_iY_i points resulting from two complete travels of $X_{i-1}Y_{i-1}$ on its rectangular path will be: 00, 01, 01, 11, 11, 10, 10, 00, 00.

master, while the X_{i-1} state determines whether the slave shall be like or unlike the master in the ith stage. Thus, the cause and effect relationship between one stage and the next described by Figs. 1 and 2 may be illustrated succinctly by Fig. 3, which shows which toggle of any stage is master, depending upon the state of the preceding Y toggle, and whether the slave shall be like ("0") or unlike ("1") the master, depending on the state of the preceding X toggle.[8] It is immediately apparent that there are eight ways of establishing the stage-to-stage causality. The next phase of this discussion will determine the various counting codes represented by the sequence of X and Y states during each of the eight possible counting operations.

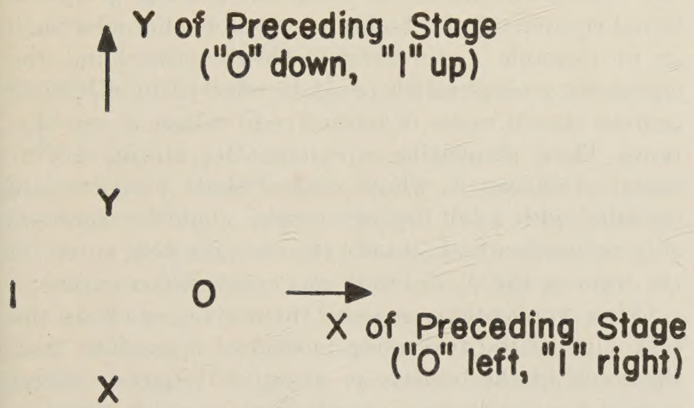

Fig. 3—Simple diagram of cause and effect between stages.

Inspection of Fig. 3 indicates that a counterclockwise succession of states in the $X_{i-1}Y_{i-1}$ plane is characterized by a $\frac{1}{4}$ cycle lead[9] of the X_{i-1} toggle with respect to the Y_{i-1} toggle, and that the leading toggle in the ith stage will be the one which demands likeness when it is master; *i.e.*, the one followed by a zero, when Fig. 3 is traversed counterclockwise. It follows that the cyclical order of the states will be the same in successive stages when the order X–0–Y–1 is counterclockwise, whereas they will alternate when the order X–0–Y–1 is clockwise.

It will be noted that one of the toggles will change whenever there is a change in a toggle of the preceding stage which causes a 0–1 or a 1–0 transition in Fig. 3 (the X toggle for the case shown). This is a property of the binary code, and the code exhibited by the 0–1 axis toggles will be a binary code, whenever it is the same toggle transition in any one stage which causes the homologous toggle in the next stage to change; *i.e.*, whenever the transitions, which cause transitions in the homologous toggle in the next stage, have like directions in all stages, corresponding, as was seen above, to a counterclockwise X–0–Y–1 order. Otherwise, the code formed will be the binary code in which the alternate binary digits are added 1 (mod. 2), and will be termed "altered binary." The binary code will read up for clockwise state transitions whenever it is the 1–0 transition which causes the next 0–1 axis toggle to change, and will be reversed and read down otherwise.

Following Ware's nomenclature, and designating by T (for true) the toggles in the 0–1 axis and by F (for false) the others, the state of the toggles in the $(i-1)$st and the ith stage are bound by the condition

$$F_i + T_i + T_{i-1} \equiv C \text{ (mod. 2)} \tag{1}$$

where C designates which of 0 or 1 is at the $T_{i-1}=0$ coordinate. (In Fig. 3 $T=X$, $F=Y$, $C=1$.)

Relation (1) indicates that, when $C=0$, and when T forms the binary code, the $T_n, F_n, F_{n-1}, \cdots, F_1$ ensemble forms an $n+1$ digit Gray code, when there are n stages (F_1 is not determined by the nonexistent T_0, but, together with T_1, determines what T_0 would have been had there been a preceding 0th stage). When $C=1$, and when T forms the binary code, the code obtained for F will be the Gray code, to all binary digits of which 1 has been added (mod. 2) and will be termed the reentered Gray code.

Likewise, when $C=0$, and when T forms the altered binary code, the reentered Gray code will also be obtained for F, whereas the Gray code is obtained for F from the altered binary code of T when $C=1$.

Except for the inclusion of T_n, the Gray and reentered Gray codes thus obtained correspond to the False Rank numbers of Brown, which, in turn, correspond to those of Ware, with the further exception of the binary digit of lowest rank, because Ware does not tabulate what Brown terms $\frac{1}{2}$ counts.

The several codes which can be obtained with the eight possible state-to-state connections can be deduced from the preceding discussion and have been tabulated in Table I. As an example, consider the fifth counter connection:

$$\begin{matrix} & 0 & \\ X & & Y, \\ & 1 & \end{matrix}$$

the detailed causal connections of which are: if $X_{i-1}=0$ and $Y_{i-1}=0$, then $\overline{X}_i \rightarrow Y_i$; if $X_{i-1}=1$ and $Y_{i-1}=0$, then $\overline{Y}_i \rightarrow X_i$; if $X_{i-1}=1$ and $Y_{i-1}=1$, then $Y_i \rightarrow X_i$; if $X_{i-1}=0$ and $Y_{i-1}=1$, then $X_i \rightarrow Y_i$. The clockwise $X0Y1$ order indicates that the XY point rotation will alternate from stage to stage, and that, together with the circumstance that the 01 axis is the Y axis, determines that the code formed by the Y axis will be the altered binary code.

[8] For instance, when $Y_{i-1}=1$, Y_i is master, regardless of the value of X_{i-1}; and, when $X_{i-1}=0$, the slave of the ith stage is unlike the master, regardless of the value of Y_{i-1}.

[9] In the successive states:

$$\begin{matrix} X = 0 & 1 & 1 & 0 & 0 & 1 \\ Y = 0 & 0 & 1 & 1 & 0 & 0 \end{matrix} \cdots X$$

will be said to lead.

TABLE I

SYNOPSIS OF BIDIRECTIONAL COUNTER CONNECTIONS AND CODES

Causality	X code	Y code	Alternating Rotations
Y 1 0 X	Binary	Reentered Gray	No
X 1 0 Y	Altered Binary	Gray	Yes
Y 0 1 X	Reversed Altered Binary	Reentered Gray	Yes
X 0 1 Y	Reversed Binary	Gray	No
0 X Y 1	Gray	Reversed Altered Binary	Yes
1 X Y 0	Gray	Reversed Binary	No
0 Y X 1	Reentered Gray	Binary	No
1 Y X 0	Reentered Gray	Altered Binary	Yes

Furthermore, we have $C=1$, because there is a 1 at the $Y=T=0$ coordinate, and, since the Y code is reversed binary, the X code will be the Gray code.

If the counter has four stages, their successive states will be as follows for an assumed input, which causes a counterclockwise rotation of the first stage, and for the initial conditions: $X_1=Y_1=X_2=X_3=X_4=0$.

$X_1=F_1$	0	1	1	0	0	1	1	0	0	1	1	0	0	1	1	0	0	1	1	0	0	1	1	0	0	1	1	0	0	1	1	0	0	←
$Y_1=T_1$	0	0	1	1	0	0	1	1	0	0	1	1	0	0	1	1	0	0	1	1	0	0	1	1	0	0	1	1	0	0	1	1	0	←
$X_2=F_2$	0	0	1	1	1	1	0	0	0	0	1	1	1	1	0	0	0	0	1	1	1	1	0	0	0	0	1	1	1	1	0	0	0	←
$Y_2=T_2$	1	1	1	1	0	0	0	0	1	1	1	1	0	0	0	0	1	1	1	1	0	0	0	0	1	1	1	1	0	0	0	0	1	←
$X_3=F_3$	0	0	0	0	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	0	0	0	0	0	←
$Y_3=T_3$	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	0	←
$X_4=F_4$	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	←
$Y_4=T_4$	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	←

Gray Code → Altered Binary Code.

Or, with separate grouping of the altered binary and Gray code digits:

Altered Binary Code				Gray Code					
Y_4	Y_3	Y_2	Y_1	Y_4	X_4	X_3	X_2	X_1	
1	0	1	0	1	0	0	0	0	
1	0	1	0	1	0	0	0	1	
1	0	1	1	1	0	0	1	1	
1	0	1	1	1	0	0	1	0	
1	0	0	0	1	0	1	1	0	
1	0	0	0	1	0	1	1	1	etc.

CONCLUSION

Brown has noted that a bidirectional counter of the type discussed here may be used to determine unambiguously[10] the position of a shaft. The logic of this counter justifies the view that true electrical gearing is realized with it and is analogous to the mechanical gearing of a binary counter with Geneva gears. Its operating speed is limited by the properties of the toggles, just as the speed of the mechanical counter is limited by the mechanical properties of its parts. The essential difference is that a mechanical counter has the memory of a miscount in the form of a broken gear. The absence of a similar memory in the electrical counter, for which an interruption of power spells the same disaster as a broken gear in a mechanical counter, is the basis for the engineer's distrust of electrical gearing in operational equipment of a highly responsible character such as, for example, a gun director. On the other hand, the enormous savings which could be effected by electrical gearing should make it attractive in a host of applications. Thus, simulating equipment for storing operational problems, in which several shaft positions are recorded with a full binary number, could be considerably reduced in bulk, if only the changes were noted, in the form of the X_1Y_1 input of a reversible counter.

Other applications suggest themselves, such as the reckoning of the traversing motion of a machine tool, the count of the positive or negative frequency difference of two oscillators, one of which may be slaved to the other much more gently than if capture had to occur within a quarter cycle, the tracking of Doppler counts to measure displacements or distances, etc.

The more complete logic of the bidirectional counter leads one to speculate as to any basic difference between the kind of problems for which unidirectional or separately instructed reversible counting only is required, and those for which bidirectional counting fulfills better the needs of the situation. A rough rationalization may lead to the view that the first are mathematical problems, and the second are physical ones.

[10] Unlike separately instructed reversible counters, selfinstructed bidirectional counters do not require that the "ripple" of a count in any one direction have terminated, before the counter may be instructed to count in the opposite direction, after which the counting operation in that new direction may proceed.

The Logical Design of a Simple General Purpose Computer*

STANLEY P. FRANKEL†

Summary—**The logical design described here is used in MINAC, partially constructed at the California Institute of Technology, and LGP-30, manufactured by Librascope Inc. These serial binary digital computers make use of magnetic drum bulk storage and use three circulating registers and fifteen flip-flops. The procedures used in performing the sixteen elementary operations are described. These descriptions indicate the circumstances in which each flip-flop or circulating register input is activated. The Boolean algebraic equations summarizing these circumstances constitute the logical design.**

Introduction

THE LOGICAL design described here was largely composed in the course of work of the Digital Computing Group of the California Institute of Technology. A breadboard model of a computer based on this logical design, called MINAC, was completed at C.I.T. in 1954 and served to check much of the design. A production version of this machine, called the LGP-30, has been completed by Librascope Inc. of Glendale, Calif. Although MINAC and LGP-30 differ in a few details of logical design the present description is substantially correct for either.

The LGP-30 has been discussed in two previous publications. One[1] describes its elementary operations and the ways in which these are used to perform complex calculations. The other[2] discussed the useful range of applications of magnetic drum computers in general, with particular reference to LGP-30. It is the purpose of the present paper to present in almost complete detail the logical design structure held in common by MINAC and LGP-30. Their constructional techniques and methods of arithmetic manipulation are described only to the extent necessary to this purpose.

Constructional Techniques

The primary memory device of MINAC is a magnetic drum. Information is held on the drum in three forms. The bulk memory is held in 64 tracks, each served by one "head" which records data in it and can subsequently read the recorded data. The information recorded in each track consists of 64 *words*, each of 32 bits (binary digits). A second type of memory of shorter access time is provided by three *circulating registers*, each consisting of a recording head and one or more reading heads following it (in the sense of drum rotation) in the same track. The time during which the 32 bits of a word are presented by a head of the bulk memory is called a *word period*. The time elapsing between the recording of a digit in a circulating register and its presentation by a reading head is about 32 digit periods so as to permit recirculation of information in one word period. The third form of information storage on the drum is represented by the *timing tracks*. Each of these is served by a single reading head which reads permanently recorded information determined only by the angular position of the drum. The digits presented by three timing tracks are combined to form various timing signals, denoted t, u, v, x, y, z. These are shown in Fig. 1.

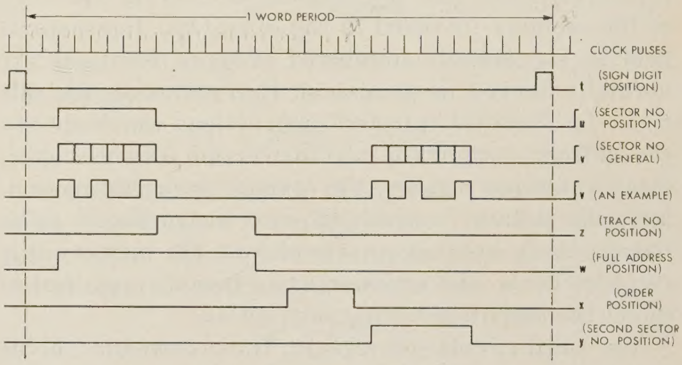

Fig. 1—Signals derived from the timing tracks.

Information which must be presented continuously over many digit periods is held in *toggles* (flip-flop circuits). Each of these can be set to one or the other of two stable states, designated 1 and 0, at the end of each digit period. The logical design consists primarily of the specification of the circumstances under which each toggle is set to 1 or to 0. If neither input is activated the toggle retains its prior setting during the next digit period. The logical design also specifies the digit recorded in each circulating register in each digit period and whether a digit is to be recorded in the bulk memory and, if so, what digit and in which track.

The input and output of data are mediated by a Flexowriter, a punched paper tape controlled typewriter. In the input process each character read from the tape sets some of the MINAC toggles. In output the state of the toggles controls the firing of a set of thyratrons which effect the closure of the relays by which the Flexowriter is operated.

* Manuscript received by the PGEC, June 1, 1956; revised manuscript received October 16, 1956.

† 1764 Redondo Ave., Long Beach, Calif.

[1] S. Frankel and J. Cass, "The Librascope general purpose computer, LGP-30," *Instruments and Automation*, vol. 29, pp. 264–270; February, 1956.

[2] S. Frankel, "Useful applications of a magnetic drum computer," *Elec. Eng.*, vol. 75, pp. 634–639; July, 1956.

The logical design is realized by a *logical network*, composed primarily of resistors and crystal diodes. Its inputs are the settings of the toggles expressing the present internal state of the computer proper (as distinct from the memory held on the drum) as well as the digits being presented by the timing tracks, circulating registers, and bulk memory of the drum. Its outputs go to the recording heads of the circulating registers, to the selected head of the bulk memory (if a recording operation is in progress), to the inputs which set the toggles for the next digit period, and to the Flexowriter thyratrons. Each input or output is, for each digit period, a binary (Boolean) variable. Each input variable is presented in duplicate, *e.g.*, by wires from the two sides of the toggle. This facilitates the expression of the logical design primarily by the monotonic Boolean functions *And* and (nonexclusive) *Or* that are easily realized by diode networks.

Functional Design

The action of MINAC consists of a series of elementary operations, each performed upon one word of its memory and determined by one instruction word. An instruction word holds an *order* indicating the operation to be performed and one *address* identifying the word of the memory involved in the operation. Instructions held in successively numbered memory locations are normally obeyed in succession. Exceptions to this rule occur for "control transfer" instructions which specify the address at which the next instruction is to be sought. One circulating register, the *counter*, primarily recirculates the address in which the next instruction is to be found. As an instruction is read from the memory it is recorded in the *instruction register* where it is retained to direct the execution of that instruction.

The third circulating register, the *accumulator*, holds a number—usually the result of the last arithmetic operation. In an arithmetic operation the number held in the accumulator is combined with a number drawn from the bulk memory and the result retained in the accumulator. The accumulator normally recirculates with a period of one word period, like the counter and instruction register. During the performance of a multiplication or division the capacity of the accumulator is increased to two word periods by the use of a second reading head.

Sixteen elementary operations are provided, as shown in Table I. The arithmetic operations act upon signed (algebraic) numbers, represented in binary expansion as described below.

Requirements for Continuous Memory

Several phases of the operation of the computer, each terminated at the end of a word period, are to be distinguished: in phase 1 (abbreviated $\phi 1$) the instruction next to be obeyed is sought. This requires selecting the appropriate track and waiting for the desired word in that track to appear. In $\phi 2$ which occupies just one

TABLE I

Instruction Order List Showing Code for Each Instruction

	Code	Instruction	Effect
Arithmetic	0001	B m*	Bring. Clear the accumulator, and add the contents of location m to it.
	1110	A m	Add contents of m to the contents of the accumulator, and retain the result in the accumulator.
	1111	S m	Subtract the contents of m from the contents of the accumulator, and retain the result in the accumulator.
	0111	M m	Multiply the number in the accumulator by the number in memory location m, terminating the result at 30 binary places.
	0110	N m	Multiply the number in the accumulator by the number in m, retaining the least significant half of the product.
	0101	D m	Divide the number in the accumulator by the number in memory location m, retaining the rounded quotient in the accumulator.
	1001	E m	Extract, or logical product order, *i.e.*, clear the contents of the accumulator to zero in those bit positions occupied by zeros in m.
Transfer Control	1010	U m	Transfer control to m unconditionally, *i.e.*, get the next instruction from m.
	1011	T m	Test, or conditional transfer. Transfer control to m only if the number in the accumulator is negative.
Record	1100	H m	Hold. Store contents of the accumulator in m, retaining the number in the accumulator.
	1101	C m	Clear. Store contents of the accumulator in m and clear the accumulator.
	0010	Y m	Store only the address part of the word in the accumulator in memory location m, leaving the rest of the word undisturbed in memory.
	0011	R m	Return address. Add "one" to the address held in the counter register (C) and record in the address portion of the instruction in memory location m. The counter register normally holds the address of the next instruction to be executed.
Misc.	0100	I	Input. Fill the accumulator from the Flexowriter.
	1000	P †	Print a Flexowriter symbol. The symbol is denoted by the track number part of the address (x).
	0000	Z †	Stop. Contingent on five switch ($T_1 \cdots T_5$) settings on the control panel.

* The address part of the instruction is denoted by m when it refers to a memory location, by † when only the track number is significant. For example, m might be 4732, meaning Sector 32 of track 47.

word period the instruction word is set into the instruction register. In $\phi 3$ the *operand word* (*i.e.*, the word in the bulk memory designated by the address then held in the instruction register) is sought by a process similar to that of $\phi 1$. In $\phi 4$, which lasts for one word period, the operation is executed, except for the prolonged operations, multiplication and division. For these the execution extends into phases 5, 6, 7, and 8. These extend the time for execution somewhat beyond the time for one drum revolution.

Except in prolonged operations the phases are distinguished by two toggles, named F and G. Phases 5 to 8 are distinguished from phases 1 to 4 by the use of a third toggle, H.

While an instruction or an operand word is being read (or written) the appropriate track of the bulk memory must be selected. Six toggles, named P_1, $P_2, \cdots, P_6$, perform this selection. They are set serially during phases 1 and 3, then remain unchanged during the word period in which the track selection must be exercised.

In a similar fashion, the order must be continuously in evidence during phases 4 to 8. Since $16 = 2^4$ orders are to be distinguished, four toggles suffice to mark them. They are denoted Q_1, Q_2, Q_3, Q_4.

Two more toggles are used, K and L. The primary duty of L is to hold carry digits in addition and subtraction processes. (Since these operations are performed serially, only one carry bit need be "remembered" in each digit period.) The search operations of phases 1 and 3 are performed with the help of toggle K, as described below.

During the execution of a multiplication or division (after $\phi 4$ in which the multiplicand or divisor is read into the instruction register) there are additional requirements for continuous memory. These requirements are met by the P toggles, which after $\phi 4$ are not needed in their track selecting capacity. The functions of the toggles are summarized in Table II.

TABLE II
TOGGLE FUNCTIONS

Name	Primary Function	Other Functions
F G H	Phase discrimination	
K	Sector search	K used for augmenting control address
L	Carry digit	
Q_1 Q_2 Q_3 Q_4	Hold order (Cf. Table I)	$Q_2 = 1$ in $\phi 1$ for blocked state
P_1 P_2 P_3 P_4	Track selection	P_1 marks odd word in periods $\phi 5$ to $\phi 8$ P_1 to P_4 hold character in input
P_5 P_6		P_5 holds sign of multiplier or divisor P_6 holds digit of multiplier or sign of remainder

THE DEVELOPMENT OF THE LOGICAL DESIGN

Except for the occurrence of prolonged operations, H stays in its 0 state, as indicated by the symbol $\mathbf{H}$. The first four phases are distinguished by the four states of F and G, as follows:

Phase	F State	G State	Symbol	Duration (word periods)
$\phi 1$	0	0	$\mathbf{FGH}$	1 or more
$\phi 2$	0	1	$\mathbf{F}G\mathbf{H}$	1
$\phi 3$	1	0	$F\mathbf{GH}$	1 or more
$\phi 4$	1	1	$FG\mathbf{H}$	1

The "product" of two or more symbols indicates the simultaneous occurrence of the indicated settings. Thus the symbol for $\phi 2$, $\mathbf{F}G\mathbf{H}$, has the value 1 only if $F=0$ (hence $\mathbf{F}=1$) *and* $G=1$ *and* $H=0$.

The last digit period of a word period is marked by a signal denoted by t, derived from the timing tracks. Since each phase change occurs at the end of a word period, the symbol t is included as a factor in each of the F and G setting equations. The phases 1 to 4 occur cyclically in the order listed. Toggle F has the state 0 during phases 1 and 2. It is set to the 1 state at the end of $\phi 2$. It holds the state 1 during $\phi 3$ and $\phi 4$, then is set to 0 as $\phi 1$ is again entered. Since $\phi 2$ and $\phi 4$ consist of only one word period each the settings of F are easily described. F is set to 1 at time t of any $\phi 2$ period, to 0 at t of a $\phi 4$ word period. The circumstances calling for setting it to 1 are denoted F', those calling for setting it to 0 are denoted $\mathbf{F}'$. (The prime here indicates the new condition of the toggle. It should not be mistaken for negation, which is here indicated by boldface.) Thus we have the two following partial equations (the + following an expression indicates that other equations show contributions to that input):

$$F' = \mathbf{F}G\mathbf{H}t +, \tag{1}$$

$$\mathbf{F}' = FG\mathbf{H}t +. \tag{2}$$

G is set to 0 on either of these two occasions on which F is changed. This may be written as

$$\mathbf{G}' = \mathbf{F}G\mathbf{H}t + FG\mathbf{H}t +.$$

The symbol + may be read as *or*. If either or both terms joined by + have the value 1 so also does the sum. By an elementary operation of logical algebra this $\mathbf{G}'$ expression may be reduced to

$$\mathbf{G}' = G\mathbf{H}t +. \tag{3}$$

(In the following no explanation of algebraic manipulations will be given.)

G is set to 1 at the ends of phases 1 and 3. The system provided for determining the durations of these phases is described below. It makes use of toggle K which will be found in the state 1 at the time t only for the last word period of either of these phases. The end of a phase 1 or 3 may thus be recognized by the occurrence of $\mathbf{GH}Kt$. Accordingly,

$$G' = \mathbf{GH}Kt +. \tag{4.1}$$

(The presence of a decimal fraction in the expression number indicates that a revision of this term is introduced below.)

The Instruction Search

In $\phi 1$ a search is conducted for the instruction whose address is being recirculated in the counter. The digits presented by the counter are denoted C. The part of the address (six bits) which determines the track selection is set up on the P toggles by a process described below. The remaining six bits of the address determine

which word of the selected track is wanted, hence the time at which $\phi 1$ should end. The six digit periods in which this *sector number* is presented by C are marked by a signal u derived from the timing tracks (cf. Fig. 1). Another timing track signal v presents a particular sequence of six digits for each of the 64 word periods of a drum revolution. In each word period it "announces" the sector number of the word period following immediately thereafter. To determine whether a word period of $\phi 1$ is to be the last word period of that phase the digits announced by v are compared with the digits presented by C during the six digit periods marked u. Agreement in all six digits calls for termination of $\phi 1$ at the end of that word period. To detect this agreement toggle K is set to 1 at the end of each word period;

$$K' = t; \tag{5}$$

thereafter disagreement sets it back to 0.

$$\mathbf{K}' = \mathbf{FGH}u(\mathbf{v}C + v\mathbf{C}) +. \tag{6.1}$$

Thus finding K in the state 1 at time t indicates that agreement has been found, as was assumed in the discussion leading to (4.1). [It is to be noted that the input described by (5) brings K to the 1 state only *after* the digit period in which it is examined in (4.1).]

The Operand Search

In $\phi 3$ a similar process is carried out, differing only in that the address of the word sought is carried in the instruction register, which presents the digits R, rather than in the counter. The two search processes are thus described by (5) and (6.2).

$$\mathbf{K}' = \mathbf{GH}u(\mathbf{v}r + v\mathbf{r}) +, \tag{6.2}$$

where r is C during $\phi 1$ and R in $\phi 3$.

$$r \equiv \underbrace{FC}_{\phi 1} + \underbrace{\mathbf{F}R}_{\phi 3}. \tag{7.1}$$

Track Selection

Like the time of entry to phases 2 and 4, the track to be selected is indicated by the address circulating in C during $\phi 1$, or R during $\phi 4$. In either case it is indicated by the digits r defined above. The six digit periods of each word period during which the track number part of an address is presented by C or R are marked by the signal z. During z in phases 1 and 3 the track number r is set into the toggles $P_1, P_2, \cdots, P_6$. For this purpose these six toggles are connected as a *shifting register;* the digits r are inserted into P_1 and passed down the chain to P_2, etc. The digit periods in which this setting takes place are denoted p;

$$p \equiv \mathbf{GH}z +. \tag{8.1}$$

During this time P_1 is set to the digit r,

$$P_1' = pr +; \qquad \mathbf{P}_1' = p\mathbf{r} +, \tag{9.1}$$

P_2 is set to the digit P_1, *etc.*

$$P_2' = pP_1 +; \qquad \mathbf{P}_2' = p\mathbf{P}_1 +, \text{ etc.} \tag{10}$$

At the end of z, P_6 holds the first (least significant) digit of the track number, P_5 the second, etc. These settings are retained for the remainder of that word period and, if that word period terminates phase 1 or 3, into the succeeding phase 2 or 4.

Order Setting

In $\phi 2$ the instruction is read from the main memory. The digits presented by the main memory are denoted V. The instruction is set into the register R during $\phi 2$ and recirculated there during the subsequent $\phi 3$. This is represented by the equation,

$$R'' = FGHV + FGHR +. \tag{11.1}$$

Here R'' denotes a digit being recorded in the instruction register. Similarly digits set into the accumulator and counter are denoted A'' and C''. (They are not toggle inputs like the singly primed symbols.) The instruction also includes a four digit order which is set into the Q toggles in $\phi 3$ in the same way as the track number is set into the P toggles. The four digit periods in which the order appears are marked by the signal x. Then

$$Q_1' = F\mathbf{GH}xR; \qquad \mathbf{Q}_1' = F\mathbf{GH}x\mathbf{R}; \tag{12}$$

$$Q_2' = F\mathbf{GH}xQ_1 +; \quad \mathbf{Q}_2' = F\mathbf{GH}x\mathbf{Q}_1 + \text{; etc.} \tag{13}$$

With a few exceptions, described below, these settings of the Q toggles are held without change until the next occurrence of a $\phi 3$.

Accumulator Input

The execution of orders in $\phi 4$ is chiefly concerned with the behavior of the accumulator. It recirculates its content without change in the first three phases; and also in $\phi 4$ on orders U, T, H, Y, R, P, and Z. As may be verified by use of Table I, these orders are collectively described by:

$$Q_1\mathbf{Q}_3\mathbf{Q}_4 + \mathbf{Q}_2(\mathbf{Q}_3 + \mathbf{Q}_4) \text{ occurs for } U, T, H, Y, R, P, Z.$$

Thus the normal recirculation of A is described by,

$$A'' = A\mathbf{H}[\mathbf{F} + \mathbf{G} + Q_1\mathbf{Q}_3\mathbf{Q}_4 + \mathbf{Q}_2(Q_3 + \mathbf{Q}_4)] + . \tag{14}$$

For the remaining orders the input to A in $\phi 4$ is as follows: on order B, A is set to V; on order E to the product AV. Together these may be described as $\mathbf{Q}_2\mathbf{Q}_3Q_4(\mathbf{Q}_1+A)V$. On orders A and S, described by $Q_1Q_2Q_3$, the output of the add-subtract mechanism, here abbreviated b, is set into the accumulator. On orders M, N, and D the accumulator content is recirculated unchanged in $\phi 4$ except, for reasons described below, for the omission of the sign digit (at time t). This input to the accumulator is described by $\mathbf{Q}_1Q_2(Q_3+Q_4)A\mathbf{t}$. In the Input process four digits have (prior to $\phi 4$) been read from the Flexowriter tape and set into the toggles, P_1, P_2, P_3, P_4. In $\phi 4$ the accumulator content is recirculated through these four toggles; P_1 following A, P_2 following P_1, *etc.*, and A'' following P_4. This contributes a term $\mathbf{Q}_1\mathbf{Q}_2\mathbf{Q}_3\mathbf{Q}_4P_4$ to A''. To induce the motion of

digits down the chain of P toggles, expression (8.1) is replaced by

$$p \equiv \mathbf{FGH}z + FG\mathbf{H}z(Q_1 + \mathbf{Q}_2 + Q_3 + Q_4) + FGH\mathbf{Q}_1Q_2\mathbf{Q}_3\mathbf{Q}_4. \quad (8)$$

For order I the last term in p produces the transfer of digits in $\phi 4$, while the parenthetical factor in the second term suppresses the usual transfer in $\phi 3$. Eq. (9.1) expressing the setting of P_1 must also be modified as

$$P_1' = pGr + pGA + ; \quad \mathbf{P}_1' = pG\mathbf{r} + pG\mathbf{A} + . \quad (9)$$

Altogether the inputs to A in phases 1 to 4 are described by (14) and by

$$A'' = AH\mathbf{Q}_1Q_2(Q_3 + Q_4)\mathbf{t} + FGH[\mathbf{Q}_2\mathbf{Q}_3\mathbf{Q}_4(\mathbf{Q}_1 + A)V + Q_1Q_2Q_3b + \mathbf{Q}_1Q_2\mathbf{Q}_3\mathbf{Q}_4P_4] + . \quad (15)$$

Instruction Register Input

After $\phi 3$ it is no longer necessary for the instruction register to retain the instruction. For the prolonged orders it is used to store the multiplicand or divisor (read from the bulk memory in $\phi 4$). Thus we change the R'' equation as follows:

$$R'' = \mathbf{FGH}V + FGHV + (G + H)R = GHV + (G + H)R. \quad (11)$$

Counter Input

In the part of each word period marked $w \equiv u + z$ the counter holds the address of the instruction next to be obeyed. This information is read, and acted upon, in $\phi 1$. To prepare for the next use of this *control address* it is augmented by unity in $\phi 2$. This operation is performed with the help of toggle K, which, as described above, is set to 1 at the end of each word period. In $\phi 2$, K is set to zero whenever the digit 0 occurs in the control address; that is, on the occurrence of $w\mathbf{C}$,

$$\mathbf{K}' = FGHw\mathbf{C} + , \quad (16.1)$$

while the counter content is complemented whenever $K = 1$.

$$C'' = FGHw(KC + \mathbf{KC}) + . \quad (17)$$

The change in control address produced by the U order is effected by transferring the content of the instruction register to the control register in $\phi 4$ on this order.

$$C'' = FGHQ_1\mathbf{Q}_2Q_3\mathbf{Q}_4R + FGH(\mathbf{Q}_1 + Q_2 + \mathbf{Q}_3 + Q_4)C + . \quad (18)$$

Test Execution

The order T is to have the same effect as U provided the sign (t) digit position of the accumulator is occupied by a 1 or if the corresponding digit of the instruction is a 1 and the *external transfer switch*, z_0, is closed. These two circumstances are expressed by $t(A + Rz_0)$. To effect the transfer the $\mathbf{Q}_4'$ equation is given the term

$$\mathbf{Q}_4' = Q_1\mathbf{Q}_2Q_3(A + Rz_0)t + , \quad (19)$$

which transforms a T into a U order in $\phi 3$. (These two orders are distinguished only by the setting of the Q_4 toggle.)

The Blocked State

To provide a way of stopping a computation a "blocked state" is introduced. This is done by making the advance from $\phi 1$ to $\phi 2$ contingent on the occurrence of $Q_2 = 1$. Then (4.1) is replaced by,

$$G' = \mathbf{GH}Kt(F + Q_2) + . \quad (4)$$

In any situation not requiring blockage Q_2 is set to 1 (or allowed to remain at 1) on entering $\phi 1$. When blockage is required Q_2 is set to 0, then $\phi 1$ lasts indefinitely. The *start button* effects a release from blockage by setting Q_2 to 1. A variety of circumstances produce blockage: the stop order, Z, induces blockage contingent on the settings of external switches and of the P toggles as set by the address accompanying the Z order. A *one-operation* switch causes blockage after each operation. An overflow in an addition or subtraction or an improper division causes blockage, so as to show that the correct result cannot be represented in the usual way. Provision is made to produce a blocked state on first turning on the computer, and as an aid in timing the Input process. All of these effects are peripheral to the operation of the computer and will not be further described here.

Addition and Subtraction

On orders A and S a sum or difference is set into the accumulator in $\phi 4$. The digits of the sum or difference will be denoted b. The Add-Subtract mechanism makes use of toggle L to hold carry digits. It has been set to 0 prior to its use in addition or subtraction. The two inputs are denoted i and j. [In subtraction the number (j), *i.e.*, the number formed by the digits j, is subtracted from (i).] In addition the carry digit, L, is set to one following the simultaneous occurrence of 1-digits in the two inputs. It is set to 0 if i and j are 0. If i and j differ the setting of L is left unchanged. Thus a carry is initiated by ij, is terminated by $\mathbf{ij}$, and is propagated by $i\mathbf{j}$ or $\mathbf{i}j$. However, L is always set to 0 at the end of the operation, after the t digit period. Thus the carry in addition is described by

$$L' = ij\mathbf{t}, \quad (20.1)$$

$$\mathbf{L}' = \mathbf{ij} + t. \quad (21.1)$$

A digit of the sum, b, is the sum modulo 2 of the digits i, j, and L. Thus

$$b \equiv \mathbf{L}i\mathbf{j} + \mathbf{Li}j + L\mathbf{ij} + Lij. \quad (22)$$

In the execution of orders A and S, occurring in $\phi 4$, the two inputs are A and V respectively. Thus

$$i \equiv A\mathbf{H} + , \quad (23)$$

$$j \equiv VH + . \quad (24)$$

These equations, together with (15), describe the performance of an addition. This process of addition is most easily understood if each number is regarded as expressed in a simple binary expansion with the least significant digit appearing first and the most significant digit appearing at time t. For example the digit at time t might be assigned the value unity, the preceding digit the value $\frac{1}{2}$, the one before that the value $\frac{1}{4}$, etc. Actually, a different system for the interpretation of numbers is normally used in this computer. It differs from this only in that the digit at time t is assigned the value -1, which permits representing signed (algebraic) numbers in the range -1 to (but not including) $+1$. Either interpretation is consistent with the above description of addition or with the process of subtraction described below. However the system for introducing blockage on an improper addition or subtraction (*i.e.*, one which produces a result beyond the capacity of the representation) is made to conform to the signed number interpretation. So also are the processes of multiplication and division.

With this signed number interpretation a number, say (x), formed of digits x is approximately the negative of the number formed from the complementary digits, $\mathbf{x}$, (where $\mathbf{x} = 1 - x$). More precisely, $(\mathbf{x})$ lacks one unit in its least significant digit to be $-(x)$. Thus if $(\mathbf{j})$ were added to (i) the result would be nearly the difference, $(i)-(j)$. By complementing i rather than j, a similarly deficient difference, $(j)-(i)$, is obtained. The correct desired difference, $(i)-(j)$, can now be obtained by complementing that sum. Accordingly the rule for subtraction is obtained from the equations above by replacing i by $\mathbf{i}$, and then complementing (22) for the sum digit. These two changes, however, bring (22) back to its original form. Thus (22) describes the result of subtraction as well as of addition, while the carry equations are replaced by

$$L' = (i\mathbf{s} + \mathbf{i}s)jt, \tag{20.2}$$

$$\mathbf{L}' = (\mathbf{i}\mathbf{s} + is)j + t. \tag{21.2}$$

Here s indicates situations in which a subtraction is performed, $\mathbf{s}$ an addition. The codes for Add and Subtract differ only in the setting of toggle Q_4, hence

$$s \equiv \mathbf{H}Q_4 + . \tag{25}$$

(In phases 5 to 8 other conditions determine s as well as i and j.)

Multiplication and Division

At the end of $\phi 4$, F and G are set to 0 as described above [(2) and (3)]. This usually initiates a $\phi 1$. However, on orders M, N, and D toggle H is set to 1 at the same time, thus producing a $\phi 5$. This is described by

$$H' = FGHt\mathbf{Q}_1Q_2(Q_3 + Q_4). \tag{26}$$

In phases 5 to 8 a succession of arithmetic processes is carried out during successive intervals of time each extending over two word periods. Toggle P_1 is used to mark off these pairs of word periods. It is set to 0 at the end of $\phi 4$, thereafter to 1 and 0 alternately. This alternation is expressed by the terms,

$$P_1' = H\mathbf{P}_1t + ; \qquad \mathbf{P}_1' = GP_1t + HP_1t + . \tag{27}$$

Phase Changes for Multiplication and Division

The marking and durations of phases 5 to 8 are as follows:

Phase	Marked	Duration
5	$\mathbf{F}GH$	2 word periods
6	$F\mathbf{GH}$	61 word periods
7	FGH	2 word periods (for M and D only)
8	$\mathbf{F}G\mathbf{H}$	1 word period (for D only)

The return to $\phi 1$ occurs after $\phi 6$ on order N, after $\phi 7$ on order M, and after $\phi 8$ for D.

The beginning of $\phi 6$ occurs after the second word period of $\phi 5$, in which $P_1 = 1$. It is indicated by the term

$$F' = \mathbf{F}GHP_1t + . \tag{28}$$

To mark the end of $\phi 6$, use is made of a part of the content of the counter, marked by the timing signal y, which is not used by the control address. In each word period the timing signal v announces a sector number during the digit periods y as well as during u, as shown in Fig. 1. This second sector number announcement is copied into the counter during each word period (hence, in particular, the last) of $\phi 3$ and held there during the subsequent phases 4, 5, and 6. This is represented by

$$C'' = \mathbf{GH}vy + (G + H)yC + . \tag{29}$$

During $\phi 6$ toggle K is used to seek agreement between v and C just as it is in $\phi 1$, except that agreement is sought during time y rather than during u. For this purpose (6.2) is replaced by

$$\mathbf{K}' = (\mathbf{GH}u + Hy)(v\mathbf{r} + \mathbf{v}r) + , \tag{6}$$

and r must now be redefined as

$$r \equiv F\mathbf{H}R + (\mathbf{F} + H)C. \tag{7}$$

Phases 4, 5, and 6 together occupy one full drum revolution. Thus the end of $\phi 6$ is marked by Kt which indicates that the sector number recorded in C during v of the last word period of $\phi 3$ has been recognized. If the order is M or D, which are distinguished from N by the presence of Q_4, $\phi 7$ is to be entered. Thus

$$G' = \mathbf{G}HKQ_4t + . \tag{30}$$

On order N the end of $\phi 6$ calls for return to $\phi 1$, produced by the terms

$$\mathbf{F}' = FHK\mathbf{Q}_4t + , \tag{31}$$

$$\mathbf{H}' = FHK\mathbf{Q}_4t + . \tag{32}$$

Phase 7 lasts for two word periods. Its end is recognized by the appearance of $FGH\mathbf{P}_1t$, which is used to set toggle F to 0.

$$\mathbf{F}' = FGH\mathbf{P}_1t + . \tag{33}$$

If the order is D this setting produces $\phi 8$. On order M, which is distinguished from D by the presence of Q_3, it is $\phi 1$ which is to be entered, hence toggles G and H must also be set to 0. Thus

$$\mathbf{G}' = FGH\mathbf{P}_1Q_3t + , \tag{34}$$

$$\mathbf{H}' = FGH\mathbf{P}_1Q_3t + . \tag{35}$$

After one word period $\phi 8$ ends and $\phi 1$ is begun, thus

$$\mathbf{G}' = \mathbf{F}GHt + , \tag{36}$$

$$\mathbf{H}' = \mathbf{F}GHt + . \tag{37}$$

Multiplication Procedure

In $\phi 4$ the operand number is picked up in the instruction register and is held there in the later phases. This number serves as the multiplicand. The previous accumulator content is kept recirculating in the accumulator and functions as the multiplier. In order to provide storage capacity for the successive partial products the accumulator is extended to slightly over twice its normal length by the use of a second reading head. The digits presented by this second head are denoted by A^*. A digit, A'', recorded in the accumulator is presented by A^* in the 65th following digit period, that is after a delay of one digit period more than two word periods. Thus information rerecorded from A^* appears every other word period but precessing by a one digit period delay per circulation. The enlarged storage capacity of the accumulator is shared by the multiplier and the growing partial product. The partial product is initially of one word length and progressively grows to about two word length. As each digit of the multiplier is used it is dropped from recirculation, hence the storage requirement of the multiplier concurrently drops from one word length to zero.

In each pair of word periods of $\phi 6$ the multiplicand, recirculating in the instruction register, is or is not added to the partial product held in the accumulator as a corresponding digit of the multiplier is 1 or 0. Most of the digits of the partial product are presented by A^* during the "odd" word periods, marked by $\mathbf{P}_1$, some however have precessed into the succeeding "even" word period. For this reason the addition process is extended to two word periods. A precaution, described below, is taken to prevent falsification of the circulating digits of the multiplier. The multiplicand is presented by R only to one word period length. It is extended to two word period length by repetition of its sign (t) digit in all digit periods of the second (even) word period.

In the process of addition or subtraction in $\phi 4$ as described above an exception to the normal behavior of toggle L is made for the t digit period. In phases 5 to 8 for multiplication (distinguished from division by Q_3) that exception is restricted to the even word periods, thus extending the process to two word periods. Eqs. (20.2) and (21.2) are now replaced by the following:

$$L' = (i\mathbf{s} + \mathbf{i}s)j(\mathbf{t} + HQ_3\mathbf{P}_1), \tag{20}$$

$$\mathbf{L}' = (\mathbf{is} + is)j + t(\mathbf{H} + \mathbf{Q}_3 + P_1). \tag{21}$$

The addition of the (extended) multiplicand in each step of the multiplication during $\phi 6$ is controlled by a digit of the multiplier held in toggle P_6 during that pair of word periods. This digit was set into P_6 in the t digit period preceding these word periods, as described by

$$P_6' = HP_1tA^*Q_3 + ; \quad \mathbf{P}_6' = HP_1t\mathbf{A}^*Q_3 + . \tag{38}$$

Similarly P_6 picks up the sign digit of the multiplier at the end of $\phi 4$ and holds it during $\phi 5$, as described by

$$P_6' = FG\mathbf{H}tA + ; \quad \mathbf{P}_6' = FG\mathbf{H}t\mathbf{A} + . \tag{39}$$

Since the action in $\phi 5$ is controlled by the sign digit of the multiplier the multiplicand is (or is not) subtracted rather than added as in $\phi 6$. Since, moreover, this is the first step of the multiplication there is no previous partial product.

The multiplicand sign is needed throughout the even word periods. It is therefore picked up by toggle P_5 at the end of $\phi 4$ and held through phases 5 to 7.

$$P_5' = FG\mathbf{H}tV + ; \quad \mathbf{P}_5' = FG\mathbf{H}t\mathbf{V} + . \tag{40}$$

In phases 5 to 7 the accumulator records the sum (or difference), b, except for the digits appearing at time t of even word periods. These are suppressed to prevent their precessing into the odd word periods. Thus

$$A'' = Hb(\mathbf{t} + \mathbf{P}_1) + . \tag{41.1}$$

The inputs to the add-subtract unit are as follows: in $\phi 5$ a subtraction is performed, thereafter additions.

$$s = \mathbf{F} \qquad \text{on } HQ_3.$$

In the routine part of the multiplication, performed in $\phi 6$, the inputs to the adder are A^* and R extended by repetition of its sign digit, P_6, during the even word period and contingent on the presence of a 1 as multiplier digit, P_6. This is expressed by,

$$i = A^*; \quad j = (\mathbf{P}_1R + P_1P_5)P_6 \qquad \text{on } FGHQ_3.$$

In $\phi 5$, in which a subtraction is done, these inputs are slightly modified. The factor, P_6, in the second term of j is omitted. This has the effect of subtracting the repeated digit, P_5, in the even word period even if the multiplier is positive. That is equivalent to depositing the digit P_5 in the small gap separating the growing partial product from the multiplier digits. If the multiplicand is negative, $P_5 = 1$, the 1-digit so deposited serves to guard the multiplier digits from erosion in the later additive steps and does no harm to the growing product. Thus for $\phi 5$ the inputs are,

$$i = A^*P_1; \quad j = \mathbf{P}_1RP_6 + P_1P_5 \qquad \text{on } \mathbf{F}GHQ_3.$$

On order N the completed less significant part of the product is recorded in the accumulator in the last word period of $\phi 6$, and the execution of the operation is then terminated. On order M a completed more significant half is recorded in the first (odd) word period of $\phi 7$.

However, to present this result in the normal form it must be delayed by one digit period. This is accomplished by adding A to itself in the even word period of $\phi 7$, after which the operation is terminated. The odd word period of $\phi 7$ is like those of $\phi 6$. Thus $\phi 7$ for multiplication is described by

$$i = A^*; \qquad j = P_5P_6 \qquad \text{on } FGHP_1Q_3,$$
$$i = A; \qquad j = A \qquad \text{on } FGH\mathbf{P}_1Q_3.$$

This description of the multiplication process may now be summarized as follows:

$$s = \mathbf{F}HQ_3 + , \tag{42}$$
$$i = HQ_3[A^*(F\mathbf{G} + P_1) + AG\mathbf{P}_1] + , \tag{43}$$
$$j = HQ_3[RP_6\mathbf{P}_1\mathbf{G} + P_1P_5(P_6 + \mathbf{F}) + AG\mathbf{P}_1] + . \tag{44}$$

Division Procedure

The procedure for division is similar to one which has been described by Burks, Goldstine, and von Neumann.[3] It is a nonrestoring system, in which each step brings the remainder toward zero by subtracting or adding the divisor as its sign agrees or disagrees with that of the remainder. It makes use of the expanded accumulator, like multiplication, to provide space for the storage of the growing set of quotient digits and to provide, by its precession, for the doubling of the previous remainder at each step. As in multiplication each step requires two word periods.

The divisor is picked up in $\phi 4$ and held thereafter in the instruction register, as described above. Its sign is held by P_5 as described by (40). The sign of the dividend is held through $\phi 5$ by P_6 as described by (39). Subsequently the sign of each remainder is set into P_6 and held for two word periods. A new remainder is formed and recorded in each odd word period. It is, however, convenient to pick up its sign in P_6 at the end of each even word period, at which time it is presented by A. Thus,

$$P_6' = HP_1tA\mathbf{Q}_3 + ; \qquad \mathbf{P}_6' = HP_1t\mathbf{A}\mathbf{Q}_3 + . \tag{45}$$

In each odd word period of phases 5 to 7 ($\phi 8$ has only an even word period) the doubled prior remainder (or for $\phi 5$ the dividend) is corrected by the subtraction or addition of the divisor (R), as the two signs held in P_5 and P_6 are alike or differ.

In $\phi 5$ the first input, i, is to be the dividend which is presented by A except for its sign digit. The sign digit is held in P_6, hence the dividend can be reconstituted as $A + P_6t$. Thus,

$$i = A + P_6t; \quad j = R, \quad s = P_5P_6 + \mathbf{P}_5\mathbf{P}_6 \quad \text{on } HF\mathbf{P}_1Q_3.$$

In the odd word periods of phases 6 and 7 the doubled remainder is presented by A^*,

$$i = A^*; \qquad j = R; \qquad s = P_5P_6 + \mathbf{P}_5\mathbf{P}_6 \qquad \text{on } HF\mathbf{P}_1Q_3.$$

In even word periods of phases 5, 6, and 7 the extended accumulator recirculates without change.

$$i = A^*; \qquad j = 0 \qquad \text{on } H(F + \mathbf{G})P_1\mathbf{Q}_3.$$

The even word period part of A^* is gradually filled by the sign digits of the remainders recorded in the odd word period. In the even (and only) word period of $\phi 8$ the digits presented by A^* consists entirely of these remainder sign digits, each of which, together with P_5, determined the direction of one of the corrections used in the progressive reduction of the remainder. The first correction was determined by the sign of the dividend, which by $\phi 8$ has precessed out of the accumulator. However, in a "proper" division the magnitude of the divisor exceeds that of the dividend, hence the sign of the first remainder must be opposite to that of the dividend. These two signs were used at an earlier stage to induce blockage on improper division by a process mentioned above (but not described in detail).

Each digit presented by A^* in $\phi 8$ is combined with P_5 to form a digit, q_p, defined by

$$q_p = A^*P_5 + \mathbf{A}^*\mathbf{P}_5$$

where q_{31} corresponds to A^* in the first digit period, q_{30} in the second, etc. to q_0 corresponding to A^* in the t digit period. Each $q_p = 1$ indicates a subtraction of the divisor, each $q_p = 0$ indicates an addition of the divisor in the progressive reduction of remainders, except that q_0 corresponds to two successive opposite corrections applied to the dividend and first remainder which, since $\phi 8$ has been reached without interrupting blockage, may be presumed to have been of opposite sign. Taking account of the doubling of the remainder at each step it can be seen that the dividend has been brought approximately to zero by the subtraction of the divisor multiplied by the following number:

$$\begin{aligned} q &= -(2q_0 - 1) + \tfrac{1}{2}(2q_0 - 1) + \tfrac{1}{4}(2q_1 - 1) + \cdots \\ &\quad + 2^{-32}(2q_{31} - 1) \\ &= -q_0 + \tfrac{1}{2}q_1 + \tfrac{1}{4}q_2 + \cdots + 2^{-31}q_{31} - 2^{-32}. \end{aligned}$$

Thus q_0, q_1, etc. are the sign digit and progressively less significant digits of an indefinitely continued true quotient in accordance with the system of number representation described above. To produce a rounded quotient of sign and 30 significant digits, the digit, q_{31}, is added to the least significant position of the number (q_p) in $\phi 8$. This digit is available in the form

$$q_{31} = P_5P_6 + \mathbf{P}_5\mathbf{P}_6$$

during $\phi 8$. Its addition to the least significant digit position is more conveniently accomplished by subtracting it from all digit positions. Thus the action in $\phi 8$ is represented by

$$i = A^*P_5 + \mathbf{A}^*\mathbf{P}_5; \quad j = P_5P_6 + \mathbf{P}_5\mathbf{P}_6; \quad s = 1 \quad \text{on } FG\mathbf{H}.$$

[3] A. Burks, H. Goldstine, and J. von Neumann, "Preliminary Discussion of the Logical Design of an Electronic Computing Instrument," Institute for Advanced Study, Princeton, pt. 1, 2nd ed. vol. 1, pp. 23–29; September 2, 1947.

The description of division may now be summarized as follows:

$$s = HQ_3(P_5P_6 + \mathbf{P_5P_6} + FG) + , \tag{46}$$

$$i = HQ_3[A^*(F + GP_1 + GP_5) + \mathbf{A^*P_5FG} + \mathbf{FP_1}(A + P_6t)] + , \tag{47}$$

$$j = H\mathbf{Q}_3R\mathbf{P}_1 + \mathbf{F}GH(P_5P_6 + \mathbf{P_5P_6}) + . \tag{48}$$

The recording of a sign digit must not be suppressed in $\phi 8$, hence (52) is replaced by

$$A'' = Hb(\mathbf{t} + \mathbf{P}_1 + \mathbf{FG}). \tag{41}$$

Record Orders

Information is recorded in the main memory during $\phi 4$ on the orders H, C, Y, and R. (Cf. Table I.) The time during which recording is performed is denoted f. On orders H and C it is all of $\phi 4$.

$$f \equiv FGQ_1Q_2\mathbf{Q}_3 + . \tag{49}$$

On orders Y and R recording is done only during the part of a word period, s, occupied by the address of an instruction. Thus

$$f \equiv FG\mathbf{Q}_1\mathbf{Q}_2Q_3s + . \tag{50}$$

The digits to be recorded will be denoted V''. On orders H, C, and Y they are the digits presented by the accumulator,

$$V'' = (Q_1 + \mathbf{Q}_4)A + . \tag{51}$$

On the order Return the address to be recorded is the second address following that of the memory location in which the R instruction was found. (The memory location immediately after that holding the R order is needed for a U order which takes control to the "subroutine" from which it is later returned as a result of the R order.) Since the counter content has already (in $\phi 2$) been advanced by one since finding the R instruction it must again be augmented by one to provide the digits V''. For this purpose toggle K is used in $\phi 4$ in the same way as in $\phi 2$. This is accomplished by omitting the factor $\mathbf{F}$ from (16.1),

$$K' = G\mathbf{H}w\mathbf{C} + . \tag{16}$$

The digits to be recorded on order R are then $(K\mathbf{C}+\mathbf{K}C)$,

$$V'' = \mathbf{Q}_1Q_4(K\mathbf{C} + \mathbf{K}C) + . \tag{52}$$

Print Order

The execution of the Print instruction, marked by the signal e, occurs in $\phi 4$.

$$e \equiv FGQ_1\mathbf{Q}_2\mathbf{Q}_3\mathbf{Q}_4. \tag{53}$$

What key of the Flexowriter is struck is determined by the state of the P toggles.

Input

The Input process takes place for the most part with the computer in its blocked state. The action of the Flexowriter on reading a tape symbol sets the Input code in the Q toggles and the digits to be inserted in the P toggles. The computer is then set into $\phi 3$, from which it proceeds to the execution of the Input "order" and then enters a blocked $\phi 1$ to await another tape symbol. A special tape symbol releases the computer from the blocked state to permit it to digest and dispose of the digits set into the accumulator under the control of an input routine.

The Complete Logical Equations

To complete the description of the logical design there remains only the assembly of the partial equations given above. The assembled equations are shown in Table III. Each equation is followed by a list of the

TABLE III

SUMMARY OF LOGICAL EQUATIONS

$F' = \mathbf{F}G\mathbf{H}t + \mathbf{FG}HP_1t$	1, 28	$\mathbf{F}' = FG\mathbf{H}t + FHK\mathbf{Q}_4t + FGH\mathbf{P}_1t$	2, 31, 33
$G' = \mathbf{GH}Kt(F+Q_2) + \mathbf{G}HKQ_4t$	4, 30	$\mathbf{G}' = G\mathbf{H}t + FGH\mathbf{P}_1Q_3t + \mathbf{F}GHt$	3, 34, 36
$H' = FG\mathbf{H}t\mathbf{Q}_1Q_2(Q_3+Q_4)$	26	$\mathbf{H}' = FHK\mathbf{Q}_4t + FGH\mathbf{P}_1Q_3t + \mathbf{F}GHt$	32, 35, 37
$K' = t$	5	$\mathbf{K}' = (\mathbf{GH}u + Hy)(v\mathbf{r} + \mathbf{v}r) + G\mathbf{H}w\mathbf{C}$	6, 16
$L' = (\mathbf{i}s + i\mathbf{s})j(\mathbf{t} + HQ_3\mathbf{P}_1)$	20	$\mathbf{L}' = (\mathbf{i}s + is)\mathbf{j} + t(\mathbf{H} + \mathbf{Q}_3 + P_1)$	21
$Q_1' = F\mathbf{GH}xR$	12	$\mathbf{Q}_1' = F\mathbf{GH}x\mathbf{R}$	12
$Q_2' = F\mathbf{GH}xQ_1$	13	$\mathbf{Q}_2' = F\mathbf{GH}x\mathbf{Q}_1$	13
$Q_3' = F\mathbf{GH}xQ_2$	13	$\mathbf{Q}_3' = F\mathbf{GH}x\mathbf{Q}_2$	13
$Q_4' = F\mathbf{GH}xQ_3$	13	$\mathbf{Q}_4' = F\mathbf{GH}x\mathbf{Q}_3 + Q_1\mathbf{Q}_2Q_3(A + Rz_0)$	13, 19
$P_1' = p\mathbf{G}r + pGA + H\mathbf{P}_1t$	9, 27	$\mathbf{P}_1' = p\mathbf{Gr} + pG\mathbf{A} + GP_1t + HP_1t$	9, 27
$P_2' = pP_1$	10	$\mathbf{P}_2' = p\mathbf{P}_1$	10
$P_3' = pP_2$	10	$\mathbf{P}_3' = p\mathbf{P}_2$	10
$P_4' = pP_3$	10	$\mathbf{P}_4' = p\mathbf{P}_3$	10
$P_5' = pP_4 + FG\mathbf{H}tV$	10, 40	$\mathbf{P}_5' = p\mathbf{P}_4 + FG\mathbf{H}t\mathbf{V}$	10, 40
$P_6' = pP_5 + HP_1tA^*Q_3 + FG\mathbf{H}tA + HP_1tA\mathbf{Q}_3$			10, 38, 39, 45
$\mathbf{P}_6' = p\mathbf{P}_5 + HP_1t\mathbf{A}^*Q_3 + FG\mathbf{H}t\mathbf{A} + HP_1t\mathbf{A}\mathbf{Q}_3$			10, 38, 39, 45
$A'' = A\mathbf{H}[\mathbf{F} + \mathbf{G} + Q_1\mathbf{Q}_3\mathbf{Q}_4 + \mathbf{Q}_2(Q_3 + \mathbf{Q}_4) + \mathbf{Q}_1Q_2(Q_3 + Q_4)\mathbf{t}] + FG\mathbf{H}[\mathbf{Q}_2\mathbf{Q}_3Q_4(\mathbf{Q}_1 + A)V + Q_1Q_2Q_3b + \mathbf{Q}_1Q_2\mathbf{Q}_3\mathbf{Q}_4P_4] + Hb(\mathbf{t} + \mathbf{P}_1 + \mathbf{FG})$			14, 15, 41
$C'' = \mathbf{FGH}w(K\mathbf{C} + \mathbf{K}C) + FG\mathbf{H}Q_1\mathbf{Q}_2Q_3\mathbf{Q}_4R + FG\mathbf{H}(\mathbf{Q}_1 + Q_2 + \mathbf{Q}_3 + Q_4)C + \mathbf{GH}vy + (G+H)yC$			17, 18, 29
$V'' = (Q_1 + \mathbf{Q}_4)A + \mathbf{Q}_1Q_4(K\mathbf{C} + \mathbf{K}C)$	51, 52	$R'' = G\mathbf{H}V + (\mathbf{G} + H)R$	11
$b = Li\mathbf{j} + L\mathbf{i}j + \mathbf{L}ij + \mathbf{Lij}$	22	$r = FHR + (\mathbf{F} + H)C$	7
$f = FGQ_1Q_2\mathbf{Q}_3 + FG\mathbf{Q}_1\mathbf{Q}_2Q_3s$	49, 50	$e = GFQ_1\mathbf{Q}_2\mathbf{Q}_3\mathbf{Q}_4$	53
$i = A\mathbf{H} + HQ_3[A^*(FG + P_1) + AG\mathbf{P}_1] + H\mathbf{Q}_3[A^*(F + \mathbf{G}P_1 + GP_5) + \mathbf{A}^*\mathbf{P}_5\mathbf{FG} + \mathbf{FP}_1(A + P_6t)]$			23, 43, 47
$j = V\mathbf{H} + HQ_3[RP_6\mathbf{P}_1\mathbf{G} + P_1P_5(P_6 + \mathbf{F}) + AG\mathbf{P}_1] + H\mathbf{Q}_3R\mathbf{P}_1 + \mathbf{F}GH(P_5P_6 + \mathbf{P}_5\mathbf{P}_6)$			24, 44, 48
$s = \mathbf{H}Q_4 + \mathbf{F}HQ_3 + H\mathbf{Q}_3(P_5P_6 + \mathbf{P}_5\mathbf{P}_6 + FG)$			25, 42, 46
$p = \mathbf{FGH}z + \mathbf{FGH}z(Q_1 + \mathbf{Q}_2 + Q_3 + Q_4) + FG\mathbf{H}\mathbf{Q}_1Q_2\mathbf{Q}_3\mathbf{Q}_4$			8

partial equations drawn from the text above which compose it. A few equations have been simplified by elementary algebraic manipulation, but no attempt has been made to reduce the equations to a most compact form or to indicate the many constructional simplifications which can be found by algebraic manipulation of this description of the logical design.

The set of logical equations shown in Table III omits a number of features of the LGP-30 structure which can conveniently be described separately: the entire system for the induction of and relase from the blocked state has been omitted. So also has the setting of the P and Q toggles in the Input process. Various devices, not described here, permit the operator to check on the functioning of the computer or to control its action without reliance on instructions already stored in the memory. These devices are necessary, although auxiliary, since the above description provides no way of inserting the input routine into the memory. The formation of t, u, v, x, y, and z from the three timing tracks is not shown. On orders U and T, which make no use of an operand word, $\phi 3$ is limited to one word period by a means not shown. The recording of a 0 in the spacer bit is ensured in a way not shown.

Acknowledgment

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A Transistor-Driven Magnetic-Core Memory*

E. LEROY YOUNKER†

Summary—**A transistor-driven magnetic-core memory which has a capacity of 1024 18-bit words has been built and is being studied. Both the read and write operations employ the coincident-current technique. The memory-drive currents are developed by transistors and the desired memory location is selected by magnetic-core selection switches. Eighteen thousand, four hundred and thirty-two memory cores are used in the storage array, 48 switching cores are used in the selection switches, and 160 transistors are used in core-driving circuits and read-out amplifiers. A typical memory cycle, reading followed immediately by writing, requires 20 microseconds.**

Introduction

IN THE FEW years since the use of square-hysteresis-loop magnetic cores in memory devices was proposed[1] the magnetic-core memory has established itself as a very attractive memory device for digital computers. Among its virtues are excellent reliability, capability of high-speed operation, and possibility of large storage capacity in compact size. The circuits associated with most present-day core memories use vacuum tubes, which add substantially to the size and power consumption of the over-all memory system. The use of transistors with a magnetic-core memory makes possible the realization of an all-solid-state memory system in which the associated circuits are compatible with the core storage array in reliability, speed, compactness, and power consumption. This paper describes an 18,000-bit coincident-current magnetic core memory which is operated entirely by transistors. This memory has been built as part of a feasibility study of transistorized magnetic-core memories by the TRADIC[2] (Transistor Airborne Digital Computer) group at Bell Telephone Laboratories. The memory is described in enough detail to show where transistors are used and what requirements are imposed on them. Detailed transistor circuits are shown and experimental results are discussed.

Description of Memory

Description of Digit Planes

In the construction of magnetic-core storage arrays, the individual cores are commonly mounted in square or rectangular mechanical assemblies. Since each core in such an assembly usually stores one binary digit of a number, the assembly is called a digit plane. The TRADIC memory is designed to store 18-bit numbers, so 18 digit planes are required. The memory can store 1024 numbers; consequently, each digit plane contains 1024 cores.

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[1] J. W. Forrester, "Digital information storage in three dimensions using magnetic cores," *J. Appl. Phys.*, vol. 22, pp. 44–48; January, 1951.

J. A. Rajchman, "Static magnetic matrix memory and switching circuits," *RCA Rev.*, vol. 8, pp. 183–201; June, 1952.

[2] Work supported by Contract AF33(600)-21536, U. S. Air Force, Air Materiel Command.

A digit plane of the TRADIC memory is shown in Fig. 1. The 1024 cores, each 0.080 inch OD, 0.050 inch ID, and 0.025 inch thick, are arranged in a rectangular pattern, 64 inches long by 16 inches wide. The photograph shows only one-half of the cores, because the assemblage of cores is folded over a center supporting plate. Notice the enlarged portion of the array which has been inserted into the upper part of Fig. 1.

Close examination would show that 6 wires pass through each core—2 of them run along a row and 4 run along a column. One pair of wires (one in a row and one in a column) is used to select a core in reading. A second pair (also one row and one column) is used to select the core in writing. One of the remaining wires in the column is the output winding and the other is the digit-inhibit winding. The purpose of the digit-inhibit winding is to control the binary value of the digit inserted into the plane during the writing operation.

The digit planes were built to Bell Laboratories specifications by the International Telemeter Corporation of Los Angeles. The eighteen digit planes were assembled at Bell Laboratories to form the three-dimensional storage array shown in Fig. 2. Strapping between digit planes connects together corresponding wires in adjacent planes that are used for selecting the desired memory location. For example, for selecting the proper column in reading, there are 16 wires which start at one end of the memory, pass through all 18 digit planes, and terminate at the other end of the memory. The output and digit-inhibit wires are individual to each digit plane—their terminations are indicated in the photograph.

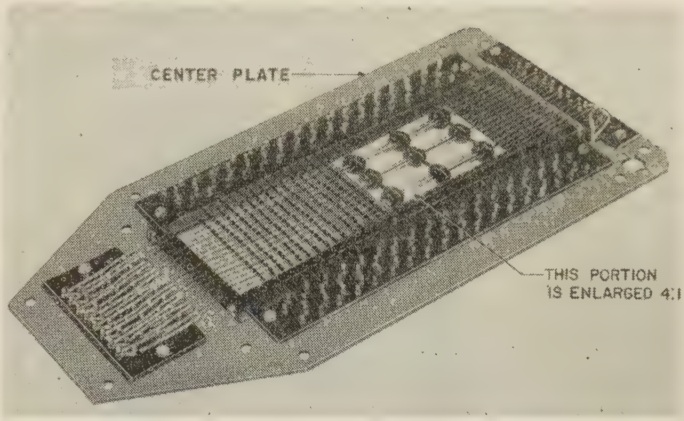

Fig. 1—Digit plane for TRADIC memory.

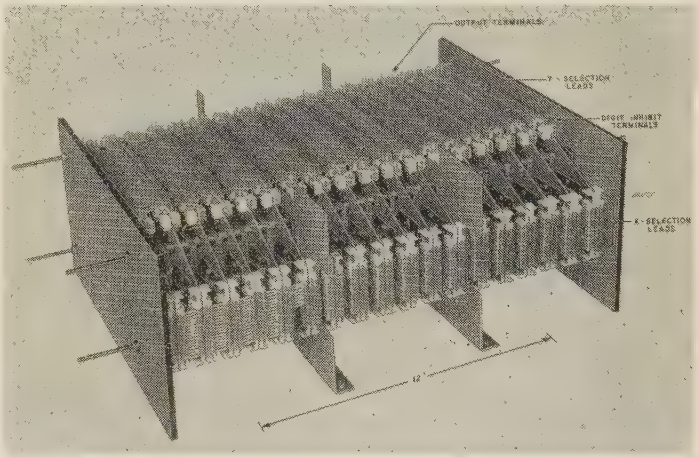

Fig. 2—Storage array for TRADIC memory.

Reading and Writing

Now let us consider the operations of reading and writing. To read a number from the memory, a current whose amplitude is one half the nominal switching current is applied to the proper row and a similar current is applied to the proper column. The polarity of the read currents is such that in each digit plane where the selected core is storing a binary ONE the core will switch and produce a voltage in the output winding. In the digit planes where the selected core is storing a ZERO, the core will not switch and essentially no voltage will appear in the output winding. Thus, the stored number appears in parallel form on the output windings of 18 digit planes.

To write a number into the memory, the desired location is selected by a coincidence of half currents on the proper row and column, as in reading. The polarity of the write currents is such that the selected core would be switched to the state of magnetization which represents a ONE.

Whether or not the core actually is switched is determined individually for each digit plane by the current in the digit-inhibit winding. The digit-inhibit winding is individual to a digit plane and passes through every core in that plane. In each digit plane where a ONE is to be written, no current flows in the digit-inhibit winding and the selected core is switched. In each plane where a ZERO is to be written, a half current whose polarity is opposite that of the write current flows in the digit-inhibit winding. One of the write currents is cancelled; the selected core does not get enough drive to switch and so stays in the state of magnetization which represents ZERO.

Selection of Memory Location

Memory locations can be selected in any order. During each read and write operation, the desired row and column in the storage array are selected by magnetic-core selection switches.[3] These switches operate in a two-phase manner. First, a switch is set to the desired position as determined by the number in the address register.

Second, the read (or write) current pulse is applied to the switch. This current flows through the switch into the selected row or column and at the same time resets the switch to a reference position. Separate switches are used to select the row and column in the reading and writing operations.

[3] M. Karnaugh, "Pulse-switching circuits using magnetic cores," Proc. IRE, vol. 43, pp. 570–584; May, 1955.

Timing in the Memory

The switching time of the magnetic cores in the storage array, which is about 4 microseconds, determines to a large extent the length of memory timing signals and the duration of the reading and writing operations.

The memory timing for one read-write cycle is shown in Fig. 3. Four general types of timing signals are used: read or write, digit-inhibit, strobe, and set-selection-switch. The read current applied to a column (long dimension of a digit plane) precedes the read current applied to a row by 2 microseconds. This is done to allow time for the disturbance caused by the column read current to die out before the row read current is applied.[4] The output of the memory is strobed by a 2-microsecond signal 2 microseconds after the coincidence of the read currents. It will be observed that the write selection switches are set during reading, and that the read selection switches are set during writing. One complete read-write cycle requires twenty microseconds.

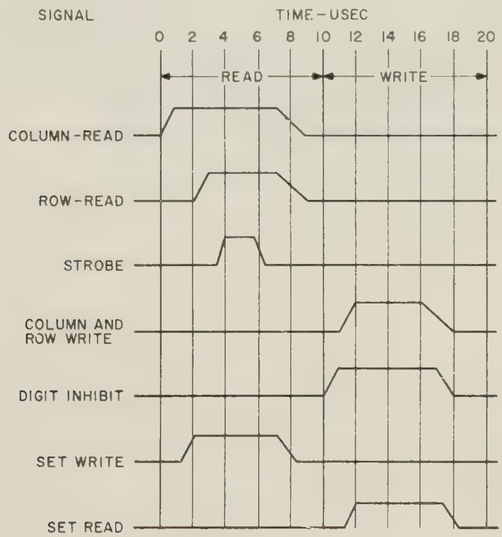

Fig. 3—Memory timing cycle.

Block Diagram of Memory

Fig. 4 shows a block diagram of the TRADIC memory. The storage array receives inputs from the selection switches and the digit-inhibit drive amplifiers, and supplies outputs to the read amplifiers. The inhibit drive and read amplifiers are provided on a per-plane basis. Only one each of the selection switches—column-read, column-write, row-read, and row-write—are provided for the entire storage array. Also only one transistor amplifier each is used to furnish the column-read current, the column-write current, the row-read current, and the row-write current for the entire array.

[4] R. Stewart-Williams, M. Rosenberg, and M. A. Alexander, "Recent advances in coincident current magnetic memory technique," unpublished paper presented at meeting of the Association for Computing Machinery at Ann Arbor, Mich.; June, 1954.

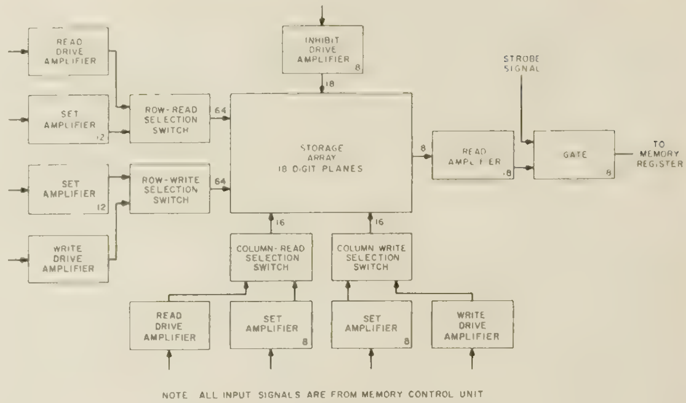

Fig. 4—Block diagram of memory.

The numbers on the lines which connect the storage array block and the adjacent blocks indicate the number of leads between units. The number inside a block indicates the required number of that unit. For example, 8 set-selection-switch amplifiers are required to set the column-write selection switch.

Detailed Transistor Circuits

In the magnetic-core memory, transistors are used to develop read and write currents, digit-inhibit currents, currents to set the magnetic-core selection switches, and to amplify the output of the digit planes. It is seen that the circuits most closely associated with a magnetic-core memory are of two types—first, circuits to provide the currents which switch magnetic cores, and, second, circuits to amplify the signal obtained from a switched memory core to a level which can drive circuits associated with the memory.

Drive Amplifiers

Amplifiers that supply current pulses to magnetic-core circuits in the selection switches or in the storage array are referred to as drive-current amplifiers. The drive amplifiers receive properly timed inputs of four milliamperes from the memory control circuits and are required to develop current pulses ranging from 70 to 200 milliamperes.

The digit-inhibit driver must supply a current pulse of about 160 milliamperes into the inhibit winding of a digit plane. The inhibit winding threads 1024 memory cores. While the inhibit-current is applied, no memory core switches, so except for small flux changes due to the nonsquareness of the memory-core hysteresis loop, the impedance of the winding is its dc resistance.

Fig. 5 shows the schematic of the digit-inhibit drive amplifier. The output transistor, Q_2, of the amplifier is essentially a switch. Normally, there is a high impedance from collector to ground and no current flows from the battery. When Q_2 is made to conduct, the collector voltage goes nearly to ground, and current flows through the digit-inhibit winding.

Now let us consider the amplifier in more detail. It uses two germanium-alloy transistors. Normally the

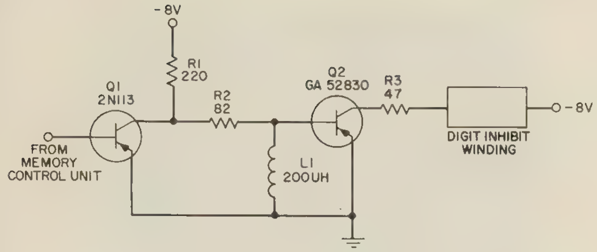

Fig. 5—Schematic of digit-inhibit drive amplifier.

transistor in the first stage, Q_1, is conducting and as a result, its collector is very near ground. The transistor in the second stage, Q_2, is cut off and no current flows through the magnetic-core load. When a digit-inhibit signal is received, Q_1 turns off and its collector starts toward -8 volts. This, of course, carries the base of the output transistor negative, and it starts to conduct. Very quickly the collector current of the output transistor reaches the value set by the limiting resistor, R_3. The base drive gradually decreases as current builds up in the inductance L_1, and the circuit is designed to provide sufficient base drive to hold Q_2 in saturation throughout the duration of the pulse. At the end of the digit-inhibit signal, the first-stage transistor starts to conduct, bringing its collector near ground. This tends to turn off the output transistor. It is turned off fast because the current flowing in the inductance, which cannot drop to zero abruptly, causes the base to go positive, back-biasing the transistor.[5]

The first-stage transistor is a germanium-alloy transistor with good high-frequency response, such as the Raytheon 2N113. The output transistor is the Western Electric GA 52830, a germanium-alloy transistor which is characterized by fast response and by good gain during large-signal operation. Its cutoff frequency is greater than 4 mc, and its grounded-emitter current gain is greater than 10, under the conditions that collector current is 200 milliamperes and the voltage between collector and emitter is no more than one quarter volt.

The waveforms for the digit-inhibit amplifier (Fig. 6) are characteristic of the drive amplifiers. The output current pulse is very nearly the same width as the input pulse and is delayed about one microsecond. The delay of the leading edge is accounted for by storage time of transistor Q_1; delay of the trailing edge is due to storage time in transistor Q_2. The turn-off drive developed by inductance L_1 [Fig. 6(c)] reduces the storage time of Q_2 by a factor of five or more.

A selection-switch-set amplifier must supply a current of about 70 milliamperes into a selection-switch set winding. The set winding consists of multiturn windings on several selection-switch cores, and since one core is switched by the drive current, the set-winding impedance has a significant inductive component.

[5] J. J. Ebers and J. L. Moll, "Large-signal behavior of junction transistors," Proc. IRE, vol. 42, pp. 1761–1772; December, 1954.
John L. Moll, "Large-signal transient response of junction transistors," Proc. IRE, vol. 42, pp. 1773–1784; December, 1954.

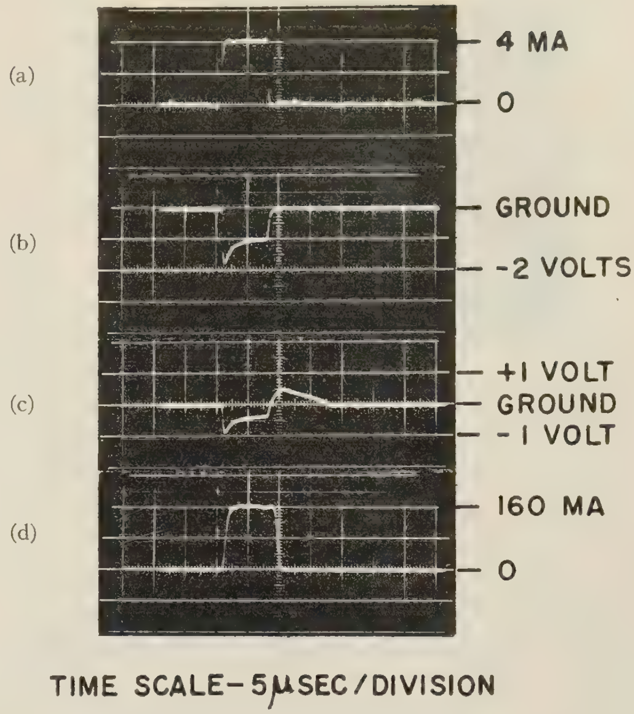

Fig. 6—Waveforms in digit-inhibit drive amplifier. (a) current into base of Q_1, (b) voltage at collector of Q_1, (c) voltage at base of Q_2, (d) collector current of Q_2.

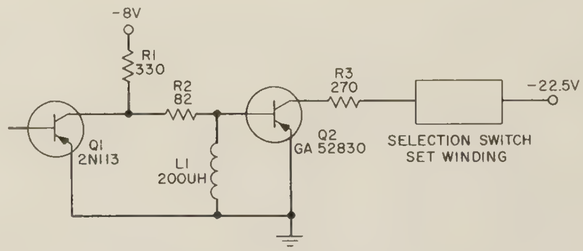

Fig. 7—Schematic of selection-switch-set amplifier.

The drive amplifiers for setting the selection switches are similar to the digit-inhibit driver. The circuit of the selection-switch-set driver appears in Fig. 7, above. Since less current is required from the output transistor in this case, the base input can be decreased. Therefore, R_1 has been increased. A more significant change is that in order to maintain a relatively constant current with the inductive load, R_3 and the supply voltage of the output stage have been increased. Waveforms for the selector-switch-set amplifier are shown in Fig. 8. The collector voltage of the output transistor [Fig. 8(a)] drops practically to ground during the output pulse; during the following overshoot, it reaches almost -30 volts. The collector current of the output transistor [Fig. 8(b)] rises rapidly at first, then gradually during switching of the core, and finally is limited by the series resistor R_3.

The memory-drive amplifier supplies the current to reset the selection switch and drives current into the storage array. It must supply 200 milliamperes into a load which contains two cores switching in the selection switch. The circuit, which is similar to the other drive

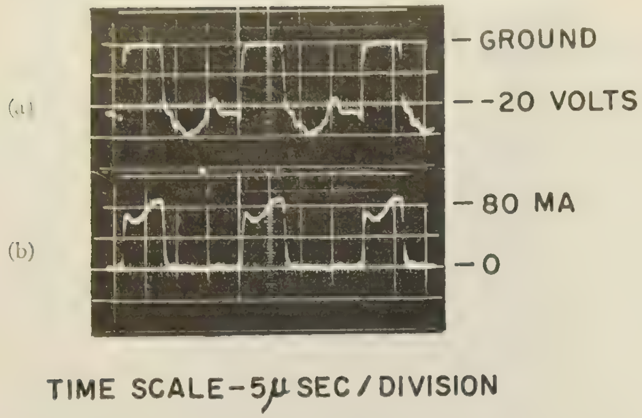

Fig. 8—Waveforms in selection-switch-set amplifier. (a) voltage at collector of Q_2, (b) current in selection-switch-set winding.

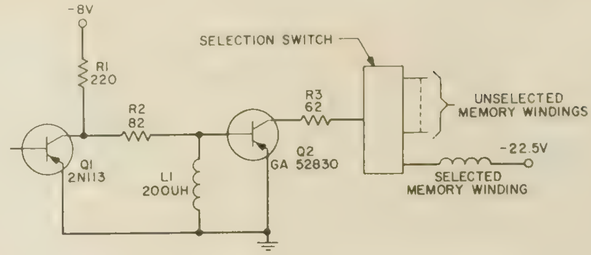

Fig. 9—Schematic of memory-drive amplifier.

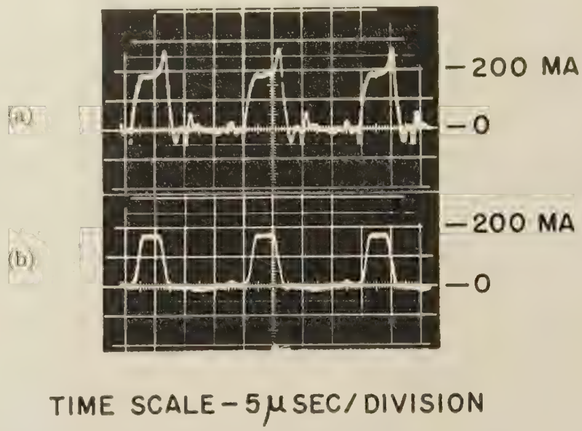

Fig. 10—Waveforms associated with magnetic-core selection switch. (a) current into selection switch from memory-drive amplifier, (b) current into selected storage-array winding.

amplifiers, is shown in Fig. 9. The waveform of the current which flows into the selection switch is shown in Fig. 10(a). The current which flows out of the selection switch into the selected coordinate of the storage array is shown by the waveform Fig. 10(b). The magnitude of this current is 170 milliamperes, has rise and fall times of 1 microsecond, and is greater than 90 per cent of its maximum value for four microseconds.

Read Amplifier

Now let us turn our attention to the read amplifier. The read amplifier must accept the output of a digit plane (about 10 millivolts) and develop an output which can control a base current of several milliamperes in Memory-Control-Unit transistors. A second requirement is imposed on the amplifier by the way the digit-plane output winding is arranged. In order to cancel spurious signals, the output winding passes through half of the cores in one direction, through the other half in the opposite direction. Therefore, the desired output signal may be either positive or negative, depending upon the direction the output winding passes through the memory core which switches. Since the polarity of the signal out of the read amplifier must always be the same, a means of inverting one polarity of digit-plane outputs must be provided.

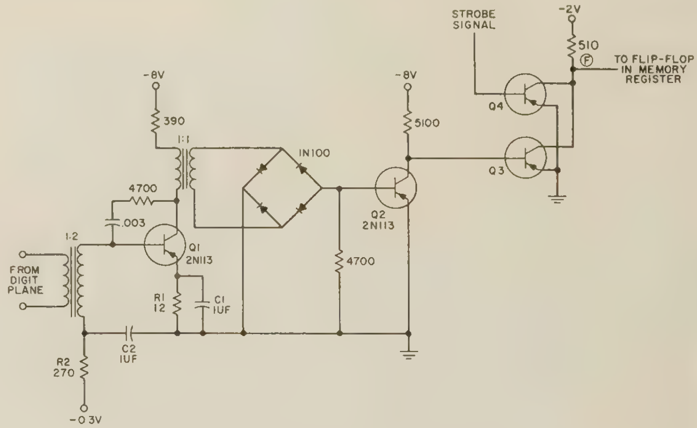

Fig. 11—Schematic of read amplifier.

Fig. 11 shows a schematic of the read amplifier. The circuit includes two transistors for amplification and four diodes for obtaining output pulses of one polarity. The digit plane is coupled to the first transistor, Q_1, by a transformer, which provides dc isolation and a voltage step-up of two to one. The emitter of first-stage transistor is grounded for signals by virtue of capacitance C_1; resistor R_1 is used to stabilize the operating point of the transistor. A small negative voltage is applied to the base of transistor Q_1 to bias it in the conducting region. The decoupling network, R_2, C_2, is used to make the first stage insensitive to small fluctuations of the ground potential which are caused by current pulses (especially digit-inhibit) in the ground system. Both positive and negative memory outputs are amplified linearly and appear at the input to the diode circuit. The diodes are arranged in a full-wave bridge rectifier with the emitter-base circuit of the second-stage transistor as the load. No matter whether the collector of first stage goes positive or negative, current flows out of the base of the second-stage transistor and makes it conduct. The collector of the second transistor goes nearly to ground and the current which before was base drive for a gate transistor now flows through Q_2. Spurious signals from the digit plane are suppressed by the nonlinear voltage-current characteristic of the diodes.

The output of the read amplifier is combined with an accurately timed "strobe" signal in the gate circuit

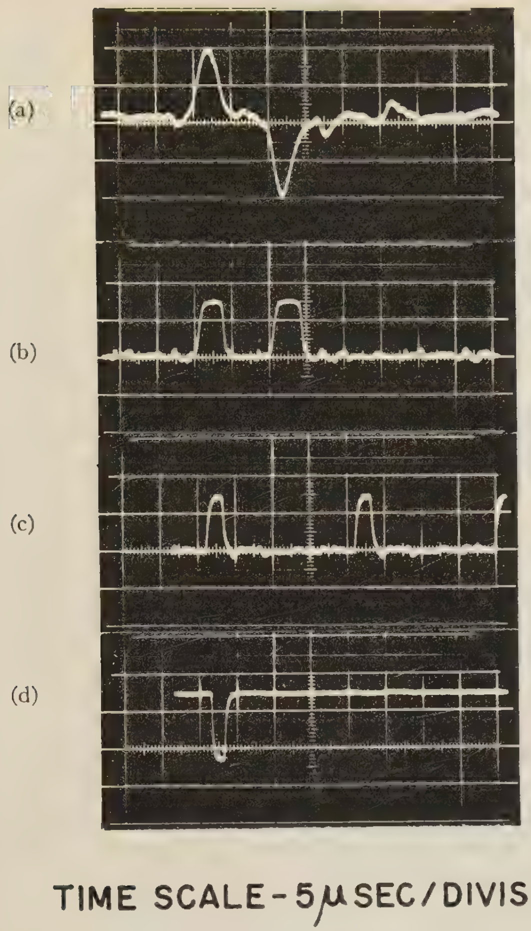

Fig. 12—Waveforms in read amplifier. (a) voltage at collector of Q_1, (b) voltage at collector of Q_3, (c) strobe signal, (d) strobed output of read amplifier.

shown at the right in Fig. 11. Normally both gate transistors are conducting and so the output point F rests near ground. In order for the voltage at this point to change, both gate transistors must be cut off. The strobe signal carries the base of one gate transistor, Q_4, to ground and cuts it off. If the output of the digit plane is a ONE, the base of the other gate transistor, Q_3, is carried to ground and it is cut off. Therefore, while both signals are applied, point F goes negative and provides the set signal for the associated flip-flop. If the output of the digit plane is a ZERO, Q_3 continues to conduct and point F stays at ground.

Operation of the read amplifier and strobe circuit for two consecutive read-write cycles is illustrated by the waveforms of Fig. 12. During the first read-write cycle, a ONE is read from the storage array and then is rewritten; during the second cycle, a ZERO is read and rewritten.

Experimental Results

Test Arrangement

Fig. 13 shows the test system which has been used to exercise the memory. Numbers can be stored in all 1024 addresses. Memory addresses are selected under the control of a 10-stage binary counter. A word generator,

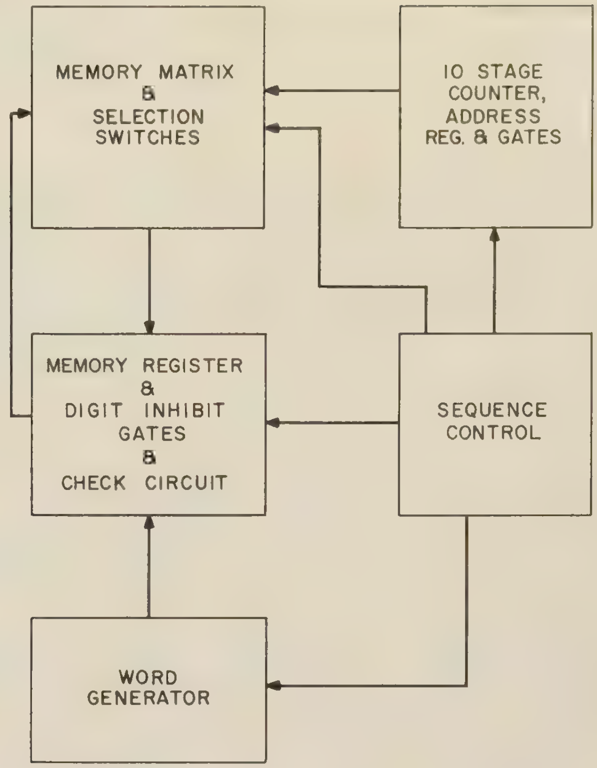

Fig. 13—Block diagram of memory-test system.

which can supply 4 hand-set 18-bit parallel numbers in sequence, is the source from which the memory is filled. Numbers read from the memory are stored in an 18-bit flip-flop (memory) register. Timing in the test system is provided by the sequence control.

The memory-test system can operate in several modes. In the "store" mode, the number at a particular address is erased by the read operation and a number set up on toggle switches in the word generator is inserted at this address on the accompanying write operation. All the addresses of the memory are filled in sequence, the same number being stored in addresses 1, 5, 9, $\cdots$, 1021. Addresses 2, 6, 10, $\cdots$, 1022 receive the same number, which, of course, can be different from the number in 1, 5, etc. In the store mode, the word generator, memory, and the memory register form an open loop, because the number read from the memory has no influence on what is written into the memory.

The "read" mode is used after the memory has been filled by the "store" process. In this case, the number read from a particular address is stored in the memory register and, on the associated write operation, is used to determine the number written into the memory. This is closed-loop operation with the memory free of the word generator.

A limitation of the read mode is that, for all addresses, the number read out is always rewritten into the same address. A more comprehensive test of the memory is provided by a combination of the store and read modes (store, read, precess) in which the four numbers set up in the word generator are made to precess through the 1024 memory address.

The memory-test system includes a check circuit which compares, bit by bit, the number read out of the memory with the number written in. Any disagreement operates an error lamp.

Marginal Checking

With the memory-test system operating in the store-read-precess mode, one voltage (or current) at a time is varied until an error is observed. Typical limiting values at which the memory operates without error are shown in Table I. It will be observed that any parameter

TABLE I

Memory Performance in Terms of Marginal Voltages and Currents

Temperature—80°F

Parameter	Maximum	Minimum	Nominal
Read and write selection currents	192 ma	150 ma	171 ma
Digit-inhibit current	198 ma	122 ma	160 ma
Drive-amplifier supply voltage			
a) Selection-switch set	−28.5v	−16.5v	−22.5v
b) Read and write	−26.5v	−19.5v	−22.5v
Read-amplifier bias voltage	−0.44v	−0.20v	− 0.32v

Note.—All parameters except the one being varied are held at nominal value.

can be varied more than ±10 per cent from its nominal value without causing an error. These data were taken when the ambient temperature was 80°F. Other experiments have shown that the memory will operate with no adjustment of voltage or current from less than 50°F to more than 100°F. The margins are substantially smaller at these temperature extremes.

Errors which occur at the marginal limits appear to be explainable in a straightforward manner. For example, the lower limit for the read- and write-selection currents is set by the type of error where a stored ONE is read out as a ZERO; the reduced drive on the memory cores results in a "turnover" voltage which is too small to be recognized reliably as a ONE signal. Similarly, the upper limit for the read and write selection currents is set by errors where a stored ZERO is read out as a ONE; the increased drive on the memory cores results in an output from half selected cores which is too large to be recognized reliably as a ZERO signal.

Conclusion

The characteristics of the transistor-driven magnetic-core memory which has been described are shown in Table II. To store the 1024 eighteen-bit numbers, it uses approximately 18,500 memory cores. To select the row and column in reading and writing, it uses 48 switch cores. To supply drive currents for the magnetic cores and to amplify the signals received from the memory, it uses 160 transistors. Sixty-two of these develop currents ranging from 70 to 200 milliamperes; the others are low-level units.

TABLE II

Memory Characteristics

Storage Capacity—1024 Eighteen-bit numbers		
Number of Magnetic Cores		
Storage array	18,432	
Selection Switches	48	
Number of Transistors	2N113	Western Electric GA-52830
Digit-inhibit amplifiers	18	18
Selection-switch-set amplifiers	40	40
Memory-drive amplifiers	4	4
Read amplifiers	36	—
Total	98	62
Power required by system	50 watts	
Time required for one read-write cycle	20 microseconds	

The voltages used in the system are 8 and 22 volts. The power consumed by the memory is less than 50 watts. A photograph of the memory system is shown in Fig. 14. Experience to date indicates that a transistor-driven memory of this kind is entirely feasible and quite attractive.

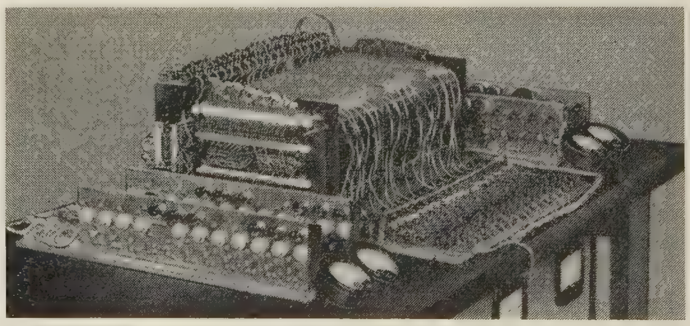

Fig. 14—Magnetic-core memory and associated transistor circuits.

Acknowledgment

The author wishes to acknowledge the contributions of his associates at Bell Laboratories, particularly A. H. Bobeck whose work has been essential to the realization of the memory described here. Thanks are also due to M. Rosenberg and V. Modlinski of International Telemeter Corporation for their cooperation during the construction and testing of the digit planes.

Current Steering in Magnetic Circuits*

J. A. RAJCHMAN† AND H. D. CRANE‡

Summary—Magnetic switches are described in which the current from an energizing source is guided or steered through one out of many possible parallel branches, the conducting branch being selected by the presetting of appropriate magnetic elements. Only a few tubes are required for energization, and the outputs, obtained with reasonable efficiency, are substantially independent of exact circuit parameters. Current steering is achieved either by core-diode combinations or by transfluxors. Decoding switches, of both types, for the selection of one out-of-many outputs according to an input code are described in detail. A current of precise amplitude of the order of amperes is switched to a selected path in microseconds. Steered decoders are ideal for addressing core memories. A commutator switch for delivering sequentially a given current to a number of loads is described. Current steering makes possible simple magnetic counters and universal code converters. Experimental results of laboratory models of decoders and commutators are given.

The principle of current steering broadens greatly the usefulness of magnetic switches by providing economy of associated electronic drivers and accuracy of switched currents.

Introduction

MAGNETIC CORES having nearly rectangular hysteresis loops have been most successful in many switching and logic circuits such as shift registers, access switches to core memories, channel selectors, coders, decoders, etc. Karnaugh[1] has reported switches in which a current from an energizing source is directed along one of a number of alternative paths to provide the output itself. This has the advantage that the amplitude and wave shape of the output depends only on the drive current source which can be regulated at will. The outputs are substantially independent of the exact parameters of the components of the network as would not be the case if they were derived directly from the induced voltages on reversing cores. Furthermore the number of tubes or transistors can be very small as these are required only for the driving sources and are not necessarily required for the generally numerous inputs of the network. Miehle, Paivinen, Wylen, and Loev[2] have also utilized the idea of directing the current in one of two parallel branches in a so-called split-winding transfer loop.

The authors have found that the principle of steering a current in one of many parallel branches of a network is most useful and can be used as a guide in the design of a great variety of circuits using magnetic elements. They have found a number of practical circuits, some of which are similar to those reported by Karnaugh.[1] This paper treats current steering as an explicit principle and describes a number of circuits not previously reported.

In the circuits referred to above, current steering is achieved by a combination of cores and diodes. It was found that current steering can also be obtained by using transfluxors.[3,4] This leads to a new class of efficient diodeless magnetic logic circuits, of which a few examples are given.

The paper includes some experimental results obtained with decoder switches both of the diode and transfluxor steered types.

Principle of Current Steering

Consider a two-terminal network with a number of parallel branches each comprising in series: a winding on a core, a diode, and a load (Fig. 1). Assume that the

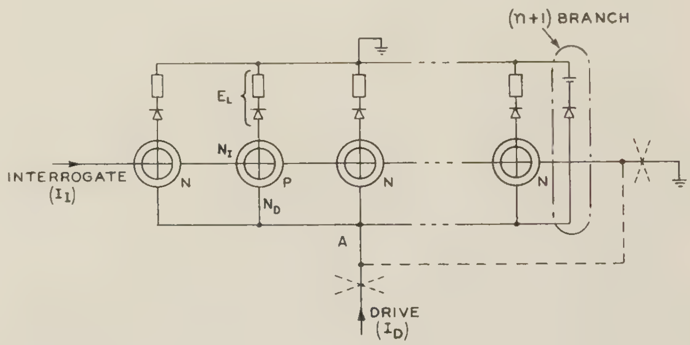

Fig. 1—Current-steering type core-diode circuit.

switching required from the circuit consists of causing current to flow in a certain load selected by the presetting of the corresponding core. The presetting, by some external means not shown on Fig. 1, causes the selected core to be in one of its remanent states P and all others to be in the other state N. The setting produces no branch currents because of the blocking effect of the back-to-back diodes.

The operation of the circuit is as follows. An "interrogate" current pulse is applied to a winding linking all cores. Polarities can be so chosen that this current will either switch over the selected core and drive the $(n-1)$ other cores merely further into saturation, or else switch-over the $(n-1)$ cores and drive the selected core further into saturation. In either case, with the proper choice of diode connections, the potential appearing on

* Manuscript received by the PGEC, October 5, 1956.
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[1] M. Karnaugh, "Pulse-switching circuits using magnetic cores," Proc. IRE, vol. 43, pp. 570–584; May, 1955.

[2] W. Miehle, J. Paivinen, J. Wylen, and D. Loev, "Bimag circuits for digital data-processing systems," 1955 IRE Convention Record, part 4, pp. 70–83.

[3] J. A. Rajchman and A. W. Lo, "The transfluxor—a magnetic gate with stored variable setting," *RCA Rev.*, vol. 16, pp. 303–311; June, 1955.

[4] J. A. Rajchman and A. W. Lo, "The transfluxor," Proc. IRE, vol. 44, pp. 321–332; March, 1956.

bus A will tend to cutoff the $(n-1)$ diodes and make the diode in the selected branch conducting. Therefore if during the interrogate period, a "drive" current is forced through the network it will be steered to flow through the selected branch only. The interrogate current is the mechanism for generating the steering voltage pattern, but by itself it causes no load currents to flow.

If certain conditions are fulfilled the steering will be complete and no current will be diverted into other branches. In the "direct"[5] steering in which the core of the selected branch switches over, the net magnetomotive force (mmf) is the difference between the mmf's due the interrogate and drive currents $(N_I I_I - N_D I_D)$ and must exceed some minimum determined by the size and coercivity of the core. The excess over this minimum determines the speed of switching and hence the generated voltage. In order to keep all other diodes nonconducting, this voltage must exceed the voltage developed across the load, E_L, plus the maximum of the disturb voltages induced on the nonselected cores. In the "complementary"[5] steering in which all but the selected core switches over, the interrogate source needs less current than for direct steering, since the drive current does not produce a counter mmf in the cores it is resetting, but must deliver, in general, more voltage since it resets $(n-1)$ rather than a single core. Complete steering is possible for either case with the proper choice of the number of turns N_I and N_D and currents I_I and I_D. For a two branch network $(n=2)$, the complementary circuit requires the same total *drive* and *interrogate* power as the direct system and is preferable because less total turns are required on the steering cores.

After the selected core has switched beyond the point where it no longer produces a sufficient voltage to steer the *drive* current completely through the selected branch, this current divides itself between the other branches. This division can be eliminated, if it is undesired, by terminating the *drive* current before the network loses its steering capability. Alternatively, additional circuitry can be used for this purpose. An example of this is also illustrated in Fig. 1 by the $(n+1)$st dummy branch, shown circled. The bias source in this branch tends to make its diode conduct, at the exclusion of all others, so that when no cores are switching the entire *drive* current is shunted through the dummy branch, and flows through the selected load only during interrogation. In practice the loadless dummy branch need not have a bias.

Steering depends on the cutoff properties of the diodes and is essentially perfect because presently available semiconductor diodes have negligible reverse currents. For all practical purposes the load current can be considered to be the *drive* current, and is independent of the *interrogate* current as long as the conditions for complete steering are fulfilled. It is interesting to compare the complementary steering circuit to one in which the saturable cores are used as controllable impedances in the conventional manner. This would be a circuit just as that of Fig. 1, but with no *interrogate* current. The *drive* current would flow preferentially through the branch including the core driven further into saturation. However, perfect steering would not result, even with the best material, since the switching core cannot represent an infinite impedance as this would require infinite unsaturated permeability and no coercivity. The additional use of the *interrogate* current makes the diode-core steerer essentially perfect as it no longer depends on the difference of impedances in the branches, but on the fact that the nonselected branches are forcefully cut off, as was explained. The diodes in the branches which provide the perfect cutoff are necessary even in the conventional circuit to permit the setting of cores without load currents. They are simply used to greater advantage in the steering circuit.

The faster the selected core switches during interrogation, the shorter the time during which the *drive* current can be completely steered, but the larger the generated voltage and hence the larger the value of current that can be steered in a given load. Therefore, within the limits of duration and amplitude imposed by the *interrogate* current, this *drive* current pulse may be of any desired shape. For example, the *drive* current can be modulated in which case its modulation will appear in the selected load at the instant of selection. Another particular example[6] consists of using for the *drive* the *interrogate* current itself. This leads to a circuit with a single current source which is of great practical importance. It is illustrated in Fig. 1 by the dashed line and two-dashed crosses which indicate how the original circuit is cut and reconnected for this mode of operation.

The current that has been steered through one-out-of many branches of a set, is available to be steered again in a second set of branches. In fact the current can be steered through many such sets of branches connected in series, as long as enough voltage swing is provided in the current source. More complex steering arrangements can be designed with series-parallel connections or interconnections between sets. Serially connected steering sets are particularly useful to drive magnetic switches based on current coincidence. Branches of several sets are made to link each element of the switch so that a particular pattern of steering through the branches produces by addition a magnetomotive force of polarity and strength required to cause switchover in only the one or more cores to be selected. Current coincidence on the windings of the selected elements is insured automatically since the same current flows serially through them. The decoders described below are examples of such switches in which there are only two branches in each serially connected set.

[5] The two steering systems are described by Karnaugh, *loc. cit.* The direct system is circuit "type AF" and the complementary is the "type AB."

[6] All of Karnaugh's circuits, *loc. cit.* are of this type.

Decoder

Tube controlled magnetic decoders have been described by one of the authors[7] in which n bivalued input signals are decoded to energize one out of 2^n outputs. Such a decoder switch for $n=3$ is shown in Fig. 2, in

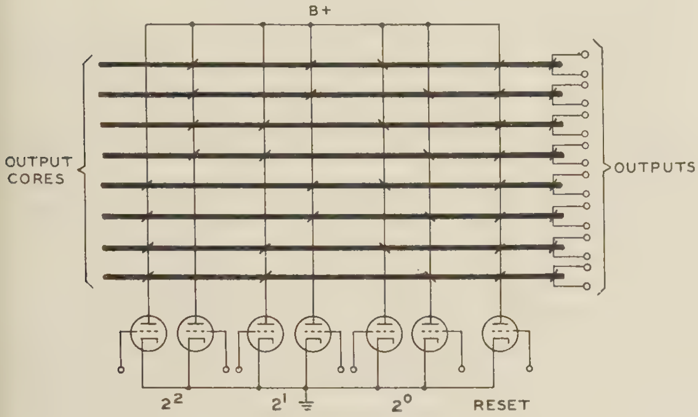

Fig. 2—Tube-controlled decoder switch.

which each heavy horizontal line schematically represents a magnetic core. The set of cores is linked by $(2n=6)$ control wires. A diagonal line at the intersection of a core and a wire indicates that the wire links that particular core (with one or a number of turns). Diagonals of different directions indicate linkages in opposite senses. One pair of wires links the cores by "halves," another by interlaced "quarters," another by interlaced "eighths," etc. One pair of wires links the cores in a direction so that current through these wires tends to switch the cores. This pair is shown in the figure as the 2^0 pair. The remaining $(n-1)$ pairs link in the opposite sense to inhibit the cores. Each pair of tubes is controlled by a single input to make one or the other tube of the pair conducting. All inputs are gated to the control tubes, so that n tubes are turned on simultaneously. For each particular combination of inputs, one and only one of the output cores is subject to switching current and switches over, all others being either inhibited or not driven. The *reset* current, applied to all cores after a previous selection, switches the selected core back to its initial state. Outputs are derived from individual windings linking each core.

A decoder switch using the current steering principle can be made by replacing each input tube by a core and diode. The output windings of the steering cores, each in series with a diode, are connected in parallel for each input pair. These pairs are all connected in series and in series with a drive source. A steering decoder is illustrated in Fig. 3, again for the case of $n=3$ inputs and of $2^n=8$ outputs. The eight output cores are represented by heavy horizontal lines as in Fig. 2, while the three pairs of steering cores are represented conventionally.

[7] J. A. Rajchman, "Static magnetic matrix memory and switching circuits," *RCA Rev.*, vol. 13, pp. 188–201; June, 1952. The binary decoding switches are described on pp. 188 and 189 under the name of "Commutator Switches."

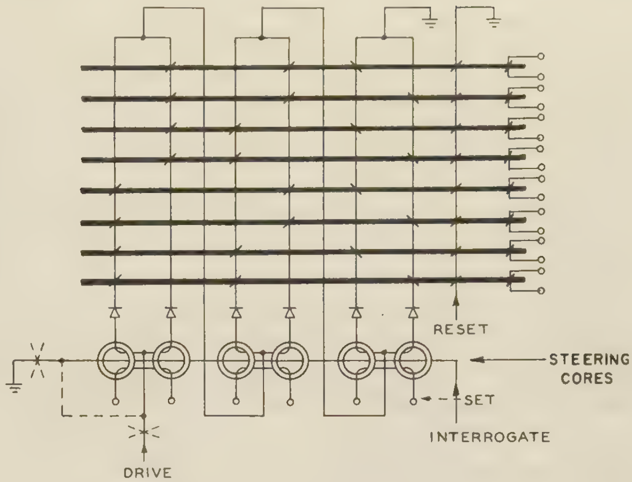

Fig. 3—Decoder with current-steering for selection.

Each input causes the two cores of a steering pair to be set in opposite states. This can be accomplished by positive or negative currents in the input *set* windings of Fig. 3 or by any other means. No currents flow as a result of these settings since all closed loops include back-to-back diodes. The inputs are stored in the steering cores and therefore need not be inserted simultaneously, but may be inserted singly or in groups.

The *interrogate* current switches one core of each steering pair and thereby predisposes to conduction one of its branches. In the "complementary" connection shown in Fig. 3, this is the branch including the non-switching core. Therefore, the *drive* current is steered in succession through the predisposed branches and acts on the output cores exactly as the tube-originated input currents of the conventional decoder and switches that particular output core which is determined by the combination of inputs.

The *reset* current is applied, as in the tube driven decoder, at any desired time after selection and returns the selected output core to its initial state.

The steering decoder has the great advantage of requiring only a single *drive* source instead of the $2n$ sources required in the conventional tube type. This not only reduces the number of sources to three (*interrogate*, *drive*, and *reset*), but insures automatically that all input branches have exactly the same currents at exactly the same time. A further reduction of the number of current sources to two can be obtained by using the *interrogate* to be also the *drive* current, as was explained previously, and is illustrated in Fig. 3 by the dashed line and crosses.

The *reset* source can also be eliminated, reducing the number of required operating current pulses to a single *interrogate-drive* pulse, because the switch resets itself automatically when this single-current pulse is of sufficient duration to divide equally in all branches after being steered. This causes a net mmf in the resetting direction on every output core which is greater than that due to the *interrogate-drive* for all practical cases

when there are four or more inputs ($n \geq 4$). This mmf resets the selected core. The interval between the selection and resetting depends on the transition between complete steering and no steering and can be controlled to some extent by the wave shape of the *interrogate-drive* pulse to be very short or have appreciable length. (For arbitrarily long intervals it is still necessary to use a separate *reset* current source.)

In the decoder described above the current steering technique is used to select an output core by the coincidence of various branch currents, but is not used to produce the actual output currents. These currents are derived from the induced voltages on output windings, in the conventional manner, so that the outputs depend critically on the characteristics of the cores and other parameters and there are disturb currents in unselected loads due to reversible flux changes. These disadvantages are not serious in most practical cases, as reasonably good and uniform cores are available. Furthermore the disturb currents can be greatly reduced by neutralizing the voltage due to reversible flux changes by identical changes induced in another core associated with each output core and identically driven. The auxiliary core is chosen to have a linear B-H relation approximating as closely as possible the B-H relation of the rectangular output core in the region of saturation.

The benefits of steered output can be obtained in the decoder by steering the *drive-interrogate* current through the branches to select an output core and steering simultaneously another *output* current to the selected output, as shown in Fig. 4. The *interrogate-drive* pulse acts as the

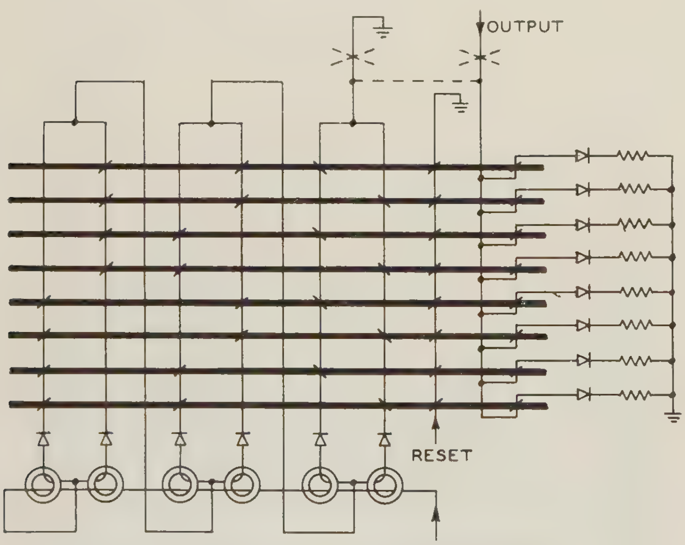

Fig. 4—Decoder with current-steering for selection and for the outputs.

"interrogator" of the output cores by selectively setting one of them, while the *output* current is the final drive. In this double steering system, the *output* current can be derived from the *interrogate-drive* by a series connection, as was done in the single steering system and as is shown by the dashed lines in Fig. 4. When this is done the single current source 1) interrogates the input steering cores, 2) sets and thereby interrogates the output cores, and 3) finally drives the selected output. The decoder with steered outputs is ideal in operation, having none of the disadvantages mentioned for the nonsteered type, but requires 2^n additional diodes.[8]

Current steered decoder switches are particularly useful for driving current coincident core memories. The binary address of the memory is decoded into the selection of one-out-of-many rows and one-out-of-many columns of the array of cores. Intense, well-regulated current pulses can be obtained in the selected lines through the use of a single tube driving both decoders. Coincidence and equal amplitude of row and column currents are therefore automatically assured. For large arrays the power of a single tube may not be sufficient, and two or more tubes may be necessary. Even in this case there will be some tube economy as fewer (though larger) tubes are required than in conventional decoders where a pair of tubes is necessary for each binary position.

Experimental Diode-Steerer Decoders

The parameters of an experimental four-input-sixteen-output decoder, illustrating a decoder of the type of Fig. 3, were as follows. The steering and output cores were rings 0.350 inch O.D., 0.220 inch I.D., and 0.120 inch H, made of square-loop ferrite of the type used for memory cores. The steering cores had interrogating windings of 2 turns, driving winding of 7 turns and also 4 turn setting windings. The circuit was of the complementary type. The selecting windings on the output cores had 2 turns. The diodes were type 1N93. Half-ohm resistances were inserted in the branches to permit current measurements. Typical results are illustrated by the photographs of oscillograph wave shapes shown on Fig. 5. For the square wave *set*, *drive*, and *reset* current

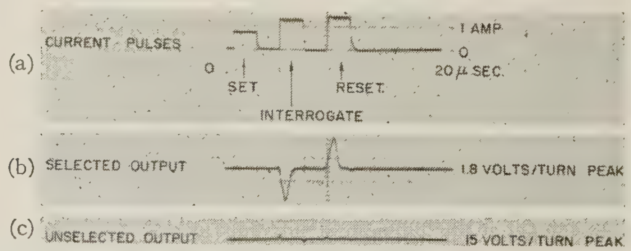

Fig. 5—Outputs of typical current-steering decoder (photo).

pulses Fig. 5(a), the voltage outputs on the selected output core are shown on Fig. 5(b), and for the unselected output core with the greatest disturbs on Fig. 5(c). The good discrimination between selected and unselected outputs is readily evident. The device was operated at about 100 kc repetition rate, but could be operated at a

[8] The switches of Figs. 3 and 4 have a similarity with switches in Figs. 10 and 13 of Karnaugh, *loc. cit.* The main difference is that current steering is used for setting (and also output in Fig. 4), while Karnaugh uses current steering for the outputs only.

higher rate particularly with air cooling of the diodes. Load currents of about an ampere were obtained.

A decoder model with 7 inputs and 128 outputs has operated successfully and has exhibited high discrimination. Much larger decoders are feasible.

Steering Encoder and Universal Switch

The steering decoder circuit can be used as an encoder, to generate m bivalued output signals according to any desired code relating them to the selection of one-out-of a number of M input signals. This is achieved by simply reversing the roles of the steering and output cores. In the switch of Fig. 3 consider that one out of the $M=8$ cores is set differently from all others. Now let the M input cores be interrogated by a current pulse through a winding linking all cores which is in series with the serially connected parallel encoding pair branches. The resetting of the selected core will induce voltages in the branch windings which will steer the *interrogate-drive* current through one branch of each pair and thereby set one or the other core of each output pair. Any desired code can be used. With the binary code shown in Fig. 3 the disturb voltages due to reversible flux changes of the unselected input cores oppose each other on the two branches of each pair and can never spoil the logic of the switch. Dummy cores can always be used to cancel any detrimental effects of these disturb voltages if there is no inherent symmetry in the code.

A decoder and an encoder can be combined into a code converter or "universal switch" to generate m output signals which can be related to n inputs according to any desired code. Fig. 6 illustrates a universal switch in

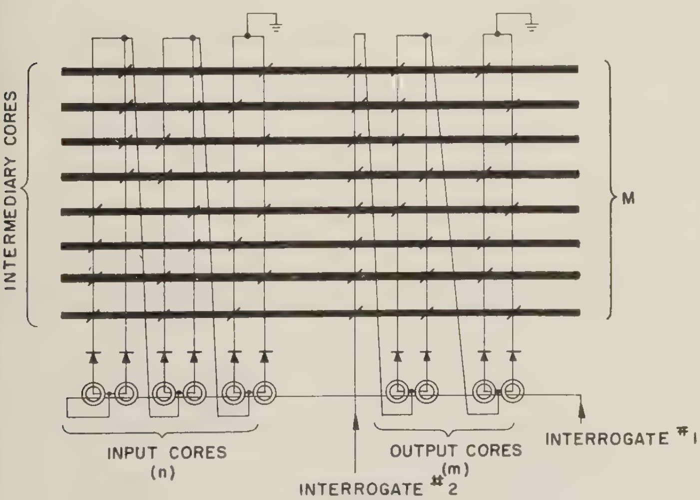

Fig. 6—Code converter or universal steering switch.

which $n=3$ and $m=2$. There are n pairs of input cores and diodes, M intermediary cores, and m pairs of output cores and diodes. The number M of intermediary cores is equal to the number of possible combinations of inputs, there being a core for every combination, and is equal to 2^m if all combinations actually occur. The branches are preferably connected in the "complementary" fashion. The switch operates in the following steps: 1) the inputs set the n pairs of input cores; 2) *interrogate* current no. 1 "interrogates" the input cores by resetting and thereby steers itself through one branch in each of the n input pairs and sets one of the M intermediary cores. This would have no effect by itself on the output cores as no currents flow in the m output branches due to the back-to-back output diodes. However, it may be convenient to use the *Interrogate* no. 1 to remove the previous setting of the output cores by deliberately linking these cores with the *interrogate* no. 1 winding. This is shown on Fig. 6. 3) *Interrogate* current no. 2 "interrogates" the M cores by resetting and thereby steers itself through one branch of each output pair and sets one core in each pair of output cores.

Counters and Commutators

In all circuits described so far current steering is used to obtain selected outputs on the basis of preset inputs. Current steering can be used also to produce a new setting on the basis of a previous one. Repeated *interrogate* pulses produce different settings in succession and thereby cause the circuit to undergo a definite cycle. The circuit becomes essentially a counter.

Consider for example a decoder-encoder circuit in which a single group of n pairs of cores is used instead of one group for the inputs and one group for the outputs as was the case in the circuit described above. The circuit has, thus, n pairs of "binary" cores and 2^n "unitary" cores as is illustrated for the case of $n=3$ on Fig. 7. The

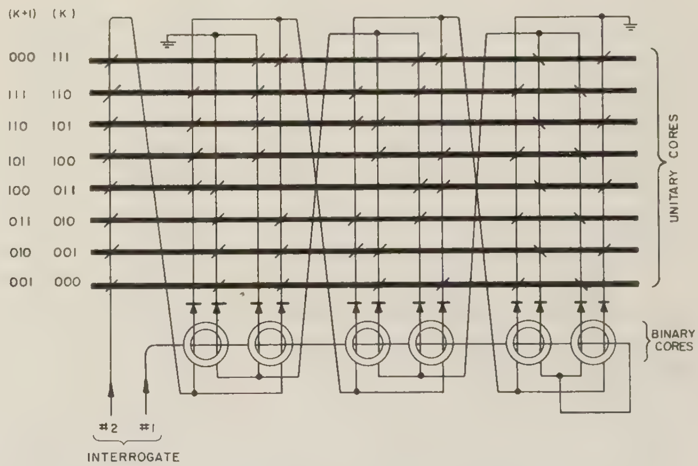

Fig. 7—Decoder-encoder counter.

circuit operates as follows. Assume that one core in each of the n pairs is set differently from the other according to some initial setting. An *interrogate* no. 1 pulse will switch over all the set binary cores and thereby steer itself through the various branches belonging to it and switch over a particular one of the unitary cores. This has the effect of decoding the binary code into the one-out-of-many unitary code. A subsequent *interrogate* no.

2 pulse applied to the unitary cores will reset the selected core and thereby steer itself through the various branches belonging to it and set one core in each of the binary pairs. This has the effect of encoding the unitary code back into the binary code. The decoding and encoding patterns can be chosen at will. For example a number k expressed as a binary number with corresponding settings of the binary cores can be decoded into selecting the kth unitary core while the encoding from the unitary to the binary code can be chosen so that resetting of the kth core causes the setting of the binary cores to correspond to the binary number $(k+1)$. With this choice of decoder and encoding patterns (shown on Fig. 7), a succession of alternate *interrogate* no. 1 and no. 2 pulses, will cause the binary as well as the unitary cores to be set in the natural succession according to the numbers $1, 2, \cdots, k, \cdots, 2^n$. Consequently, the circuit can be considered to operate either as a ring counter or as a binary counter. In its use as a ring counter, this circuit has the advantage over a conventional core-diode ring counter in that it requires, for a ring of 2^n cores, only $4n$ diodes instead of 2^n. As a binary counter, this circuit has the unusual property that the binary numbers set in the binary cores need not succeed each other in the natural order 1, 2, 3, etc., but can be in any desired one out of the (2^n) possible orders. For simplicity, the setting and output windings on the binary and unitary cores are not shown on Fig. 7.

Another example of a circuit in which new settings are produced is the "two phase stepping register" previously reported[1] which could also be thought of as a current steering commutator, Fig. 8. The purpose of the circuit is to deliver a given current in succession to a number of loads. The steering cores are divided into two groups. A first drive current, steered by a given core (k) of one group flows through a corresponding load and switches a core $(k+1)$ of the second group. In turn, a second drive current steered by the previously set core $(k+1)$ flows through its corresponding load and sets a new core $(k+2)$ in the first group and so on. The circuit is similar to the conventional magnetic shift register (used as a ring counter) with the important difference that the advance current itself is steered through the successive loads.

The advance current can be modulated, *i.e.*, the advance pulses need not have square tops nor need successive pulses be identical as long as their amplitude is sufficient for the advance action. However, to distribute modulated signals it is often convenient to separate the *drive* and *interrogate* functions. The cores are linked by another set of parallel branches which carry the loads in series with additional diodes. The additional *drive* source of modulation is steered in succession through these branches due to the action of fixed amplitudes *drive* no. 1 and *drive* no. 2 which act as the *interrogate* and *set* for the circuit. (This is not shown on Fig. 8.)

It is possible to design the commutator so that most of the energy of the driving sources appears in the load and only a small part is dissipated in the steering cores and diodes. Experimental current-steered commutator switches have been operated with 80 per cent of the drive energy appearing in the loads. Currents of one to two amperes have been steered to successive loads, in time intervals of one to a few microseconds.

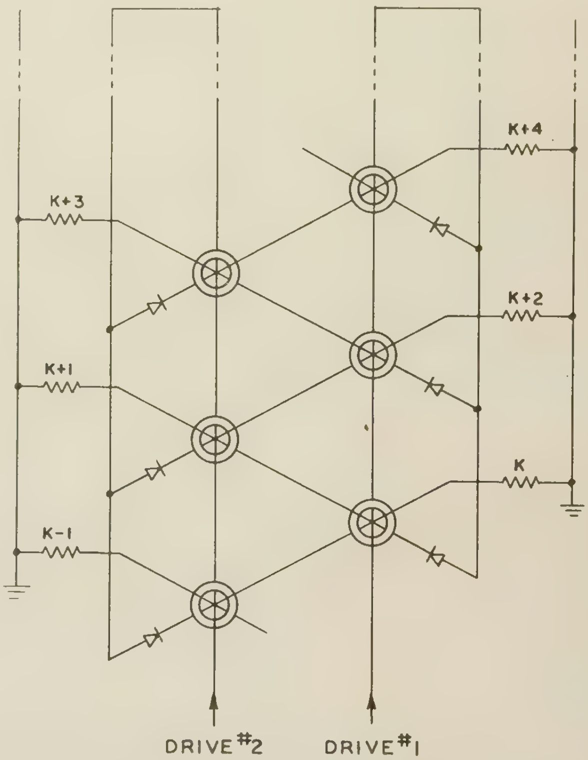

Fig. 8—Current-steering commutator.

The current steered commutator is described here anew to show the additional possibility of commutating modulated signals and to emphasize the high efficiency attainable. The circuit has a number of important applications, *e.g.*, in multiplexing systems, for sequential computers, for telemetering, etc.

Transfluxor Steering

Diodeless steering is possible by using transfluxors[3,4] instead of diodes and cores. The transfluxor is a magnetic gate with stored variable setting which in its simplest form has a core with two apertures of unequal diameter as illustrated in Fig. 9. The areas of the legs 2 and 3 are equal and that of leg 1 is equal to or greater than their sum. The basic concepts can be understood by considering the large aperture as being provided for input and storage and the small aperture for sampling and output.

A sufficiently large *block* current pulse will leave all remanent flux in a clockwise sense as indicated by the arrows of Fig. 9(b). This is defined as the blocked state, in which a moderate *drive* current of either polarity will cause no flux changes about the small aperture. A negative (opposite to arrow) *drive* current, tends to drive leg 3 further into saturation and therefore no flux is

switched no matter how intense it is. A positive *drive* current tends to reverse the flux in legs 3 and 1, and bring leg 2 further into saturation. No flux will be switched as long as the *drive* current is less than the value that creates a magnetomotive force along the path around both apertures [Fig. 9(c)] equal to the coercive force required in square loop materials to produce switch-over. For a *drive* current larger than this critical value, flux will be switched in leg 3 and leg 1. This is referred to as spurious unblocking, and is important in the transfluxor steerer.

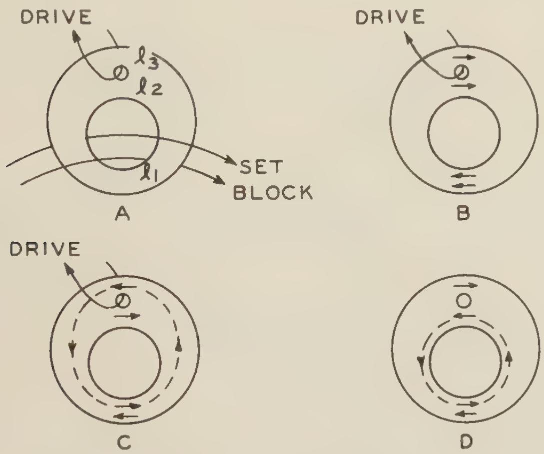

Fig. 9—Transfluxor principle.

Assume the transfluxor is blocked. A *set* current greater than some minimum value will switch some flux around the large aperture. The larger the *set* current the larger the amount of set flux. In the following it will be assumed for simplicity that the *set* current is just large enough to reverse all the flux in leg 2, although steering operations are possible also with partial settings. Ideally, no voltage is induced in the *drive* winding when the transfluxor is being *set*, since no flux is changed in leg 3. Actually there is some negligible flux change due to the imperfection of loop rectangularity. In the *set* state, flux can be reversed around the output aperture via legs 2 and 3. A positive *drive* current greater than some minimum will reverse an amount of flux depending on the excess over this minimum. All flux will be switched for a value, which with proper geometry, can be somewhat smaller than the value producing spurious unblocking via legs 3 and 1.

Transfluxor steering is achieved by the use of a transfluxor winding linking leg 3 connected in series with a branch load in each of a number of parallel branches. This is illustrated in Fig. 10 for the case of two branches. The steering action can be considered to be due to the difference in effective impedances of a blocked and set transfluxor, so that by setting the two transfluxors to different states a preferential current flow can be obtained just as in the conventional core-diode steerers using the cores as controllable impedances, mentioned earlier. However, diodes are not required since the

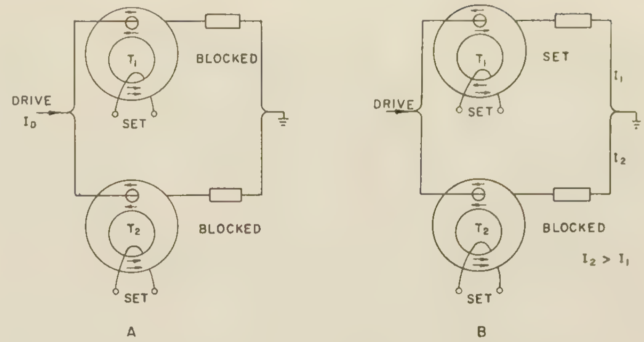

Fig. 10—Transfluxor current-steering.

setting of the transfluxors causes no voltages in the output windings.

The operation of the transfluxor steerer can be understood by following the detail of current drives and resulting flux changes. When the two transfluxors are blocked, as in Fig. 10(a), the *drive* current will not be steered, but rather be divided between the two branches, equally if the loads are equal. If one transfluxor is set, *e.g.*, T_1 in Fig. 10(b), the *drive* current I_D divides into a relatively smaller current I_1 and larger current I_2. This division results from certain flux changes in the transfluxors.

To understand the relation between I_1 and I_2 during *drive*, assume first that both branch loads are zero. Then the transfluxor output windings are directly in parallel and any voltages generated by the changing of flux in T_1 and T_2 must be equal. Consequently the total flux changed in each branch at every instant must also be equal as they occur at the same time. Since T_1 and T_2 operate on different *B-H* loops, transfluxor T_1 being set and T_2 blocked, it takes different magnitudes of current to produce equal flux changes, Fig. 11. For reasonably

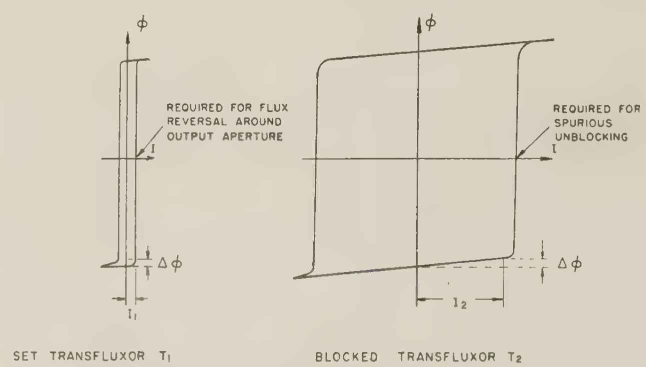

Fig. 11—Hysteresis loop of sets and blocked transfluxors.

square loop magnetic material the blocked transfluxor T_2 requires a large current I_2 to produce the same flux change that a smaller current I_1 produces in the set transfluxor T_1. The ratio of currents I_2 and I_1, is defined as the discrimination. With no loads the discrimination will remain constant in time. However, when there are loads, other than purely inductive, the currents I_1 and I_2 will eventually become equal for equal loads, and the

discrimination, initially at some high value, will asymptotically tend to unity. This results from the fact that eventually there are no longer any flux changes and the currents divide according to the load impedances. The discrimination is low for large loads since the voltages across the transfluxor windings are a small part of the total branch voltages. Consequently, the loads must be reasonably small, to obtain good discrimination.

It is interesting to consider the variations of the branch currents I_1 and I_2 as a function of time, for different *drive* currents, when there are reasonably small equal resistive loads and the transfluxor T_1 is set and T_2 blocked. Typical experimentally found variations are shown in Fig. 12. For a relatively long *drive* of magnitude less than that required for spurious unblocking, there is a period T of relatively high discrimination after which the currents approach equality [Fig. 12(a)]. The legs 3 are left in different states. Consequently during a subsequent *block* branch currents will flow. These currents are necessarily equal and opposite for the two branches. For the same magnitude of *drive*, but shorter duration, Fig. 12(b), not all possible set flux is switched and therefore smaller branch currents flow during a subsequent *block*. When the *drive* current is sufficiently large to produce spurious unblocking, the legs 3 are both left in the same state with the result that no branch currents flow during subsequent *block*, Fig. 12(c). During the time that the blocked transfluxor spuriously unblocks, the roles of the transfluxors T_1 and T_2 interchange and I_1 becomes larger than I_2 by an amount which is usually small and generally tolerable. Note that only small, negligible branch currents flow during *set*, for all cases.

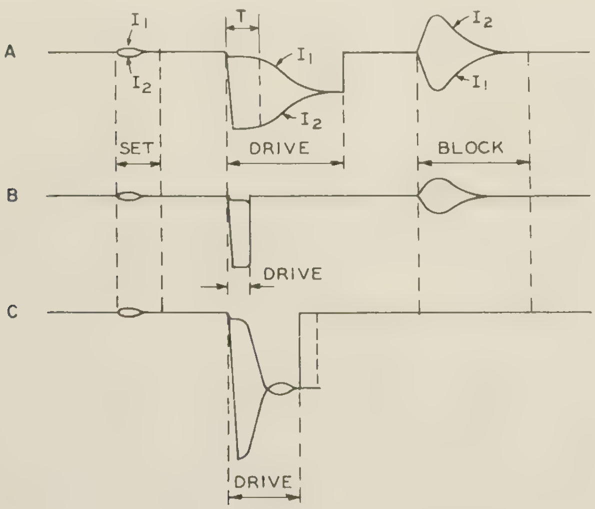

Fig. 12—Current variations in branches of transfluxor steerer.

In the operation of the transfluxor steerer, branch currents are undesirable during *set* and *block*, even in the unusual cases where the logic would permit, since they slow down these steps and consume power. As explained previously, during *set*, there are substantially no branch currents. During *block* branch currents are zero only if the flux in leg 3 of both transfluxors are either 1) reversed simultaneously with resultant opposition of induced voltages or 2) are not reversed at all. This results in two possible modes of operation.

The first mode is obtained with a *drive* current intense enough to produce spurious unblocking of the initially blocked transfluxor and thereby bringing it to the same state as that of the initially set transfluxor which has been driven. The *drive*, being intense, provides fast flux switching. This results in an inherently fast over-all operation since the *block* and *set* steps, producing only negligible branch currents, can be performed arbitrarily fast.

The second mode consists in using a pair of *drive* pulses, one *positive* and one *negative*, and is useful to obtain equal and opposite currents in each branch. The *positive drive* has a function similar to the *drive* of the first mode, but is limited to a value producing no spurious unblocking. The *negative drive* which is equal to the positive *drive*, restores the flux of leg 3 of the initially set transfluxor and causes branch currents which are equal and opposite to those flowing during the *positive drive*. A subsequent *block* causes no branch currents. It is interesting to note that *block* can be combined with *set* into a single step by simultaneously setting one transfluxor and blocking the other.

After *negative drive* the states of both transfluxors are exactly the same as after *set*. Consequently an indefinite number of *positive*, *negative drive* pairs can be used after a single set with a resultant train of positive and negative steered branch currents. At any time the resultant train of pulses can be altered according to new information by a *block-set* step. This routine operates each transfluxor in its "nondestructive" output mode. The first mode of steering, based on spurious unblocking, utilizes a "destructive" mode of transfluxor operation, in which the stored information is lost during *drive*, and is useful in the many practical cases requiring only a single steered step particularly when fast operation is desired.

An advantage in discrimination is obtained by using a *drive* winding linking both legs 2 and 3 as illustrated in Fig. 13(a). The Fig. 13(b) shows for comparison the simpler winding, used previously, linking leg 3 only. In both cases a given *drive* current will produce the same mmf around the output aperture which is proportional to $2N$, the number of turns. On the other hand, the net mmf tending to reverse the flux via legs 3 and 1, and thereby produce spurious unblocking, is proportional to $2N$ with the simpler one leg winding but proportional to only N with the two leg winding. Consequently the excursion of flux experienced in the blocked transfluxor due to imperfect loop rectangularity will be less. This results in improved discrimination. However, during *set*, voltage is induced in the two leg winding since most of the flux changes are in leg 2, and only a small part in leg 3. This voltage is reduced by the resultant current in the load circuit which tends to equalize the amount of flux set in legs 2 and 3. This current is negligible in most

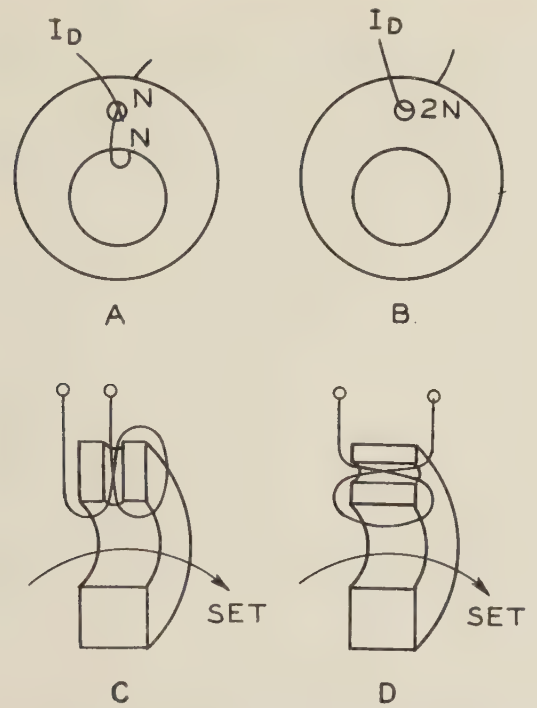

Fig. 13—(a) Output winding linking leg 2 and leg 3. (b) Orthogonal apertures.

practical cases. With an output aperture perpendicular to the setting aperture as illustrated in Fig. 13(c), the flux is divided equally between legs 2 and 3 during *set* and there is absolutely no current caused to flow in the loads. Because transfluxors of this geometry are more difficult to make and there is little resultant improvement in operation, transfluxors with parallel apertures [Fig. 13(d)] were used in all transfluxor steering experiments.

Transfluxor Steered Decoder

Transfluxor steering of current through one branch of a parallel pair can be repeated in many pairs connected in series and is directly applicable to driving a decoding switch. The example of a decoder with $n=3$ inputs and $2^n=8$ outputs used to illustrate the tube and core-diode decoders is used again in Fig. 14 to illustrate the transfluxor steering decoder. After one transfluxor in each pair is set by the inputs, the *drive* current is steered through the branch of each pair including the blocked transfluxor and thereby causes a net reversing mmf on only the single selected output core.

Because the transfluxor steering discrimination D is finite, currents are diverted into the nominally nonconducting branches and oppose the effect of the *drive* current on the selected core. The logic of the switch is not changed as long as the selected core has a net switching mmf and all other cores have no or inhibiting mmf's. It turns out that if the number of turns of the windings of the driving input pair is chosen to be $k=1+(n-2)/D$ times greater than that of the remaining $(n-1)$ inhibiting pairs, the logic of the circuit is preserved for all values of n and D and the effective driving mmf on the selected core is reduced by only a factor of $(D-1)/D$. In practice the ratio k of the number of turns on the driving and inhibiting selecting windings need not have the exact value of $1+(n-2)/D$ and can easily be obtained with a small number of turns. Even single turn on all windings, yielding $k=1$, can be used in many practical cases. While a finite discrimination is tolerable it is nevertheless desirable that it be as large as possible because it determines the effective drive. The discrimination is that much the better, the greater the ratio of voltages on the transfluxor to that across the load, as was explained previously. Steering transfluxor cores which are relatively large compared to the output cores are therefore necessary.

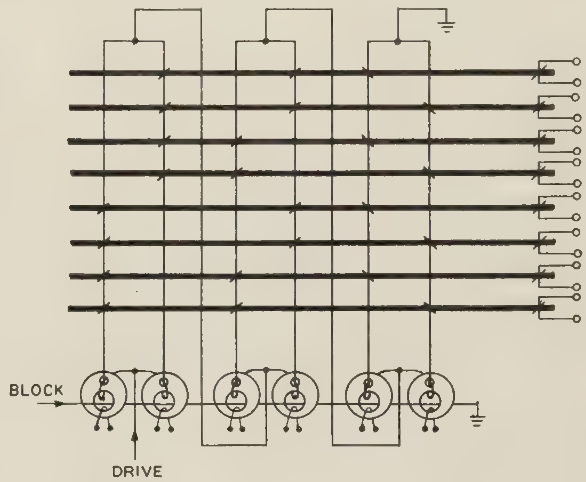

Fig. 14—Transfluxor steered decoder.

The operation of the decoder is based on the spurious unblocking mode of transfluxor steering explained above. The *drive* current is sufficiently intense to not only reverse the selected output core, but also to produce spurious transfluxor unblocking and thereby to leave all transfluxors in the same state. This intense *drive* current, left on beyond the steering period, divides itself equally in all branches and causes a net inhibiting mmf on all cores which automatically resets the selected core, eliminating thereby the need for a separate *reset* winding and a deliberate reset period. The reset mmf is greater than the drive mmf when $n \geq 4$ as was explained in connection with the diode-core steered decoder. During the *drive*, the selected output core produces a positive and a negative pulse pair; at its termination all output cores are reset and all transfluxors unblocked. A subsequent *block* pulse blocks all transfluxors preparatory to a new setting. Fast over-all operation is possible because the intense *drive* provides for: 1) very fast selection, 2) very intense resetting mmf with consequent fast resetting, 3) short period between selection and resetting and also because intense, 4) *block* and *set* pulses are not counteracted by any branch currents. Furthermore, the transfluxor steerer decoder is free from the speed limitation in diodes due to carrier storage.

In an experimental transfluxor decoder with $n=4$ inputs and $2^n=16$ outputs, the discrimination expressed as the initial ratio of branch currents was typically about 10. The transfluxors were of a laboratory type and the cores were typical ferrite switch cores. The duration of the switch-overs was short enough that the three steps of *block*, *drive*, and *set* could be accomplished all in less than two microseconds, using moderate drives.

Conclusion

The concept of steering a current through a magnetic circuit by deliberately opening all but a chosen path is extremely simple and leads to the conception of a great variety of practical circuits. The use of current steering greatly reduces the size and power of the associated electronic circuits required with most present day magnetic switches because the electronic components, no longer performing any logic, are used merely as energizing sources.

Current steering is applicable not only for on-off signals, but also for signals carrying analog information because the steering faithfully preserves current amplitude. Such perfect steering requires the use of diodes. These semiconductor devices do not limit seriously the usefulness of the circuit because they are required in reasonably small numbers, and presently available junction types can reliably handle large currents.

Steering by transfluxors requires no diodes and leads to a novel class of circuits: efficient diodeless magnetic logic circuits. Although steering is not as perfect as with diodes, these circuits have many possible applications, due to the extreme reliability of an all-magnetic circuit and due to the potential high-speed operation.

Several magnetic logic circuits have been developed in recent years, which consist of networks of gainless elements driven by a central power source. These circuits fall into two classes: voltage driven and current driven circuits. In the current steered circuits, current drive is in its purest form and permits the manipulation of analog information. The advent of transistors challenges the concept of magnetic logic with a central power source, as local sources of gain and control are easily available. It is nevertheless likely that logic magnetic circuits of the voltage, current, or steered current types, will be an important part of the electronic art for many years.

Acknowledgment

Arthur W. Lo and George R. Briggs of RCA Laboratories have contributed greatly to the ideas and various aspects of the experimental work described in this paper.

An Electronic Analog Multiplier Using Carriers*

ERICH S. WEIBEL†

Summary—**An electronic analog multiplier is described, which is based on a modulation technique. No dc amplifiers are used, which makes the output entirely free of drifts. All distortions up to the fourth order are eliminated. The experimental model that has been built handles inputs from dc to 7 kc and gives an output from dc to 14 kc. The amplitude range of the output is 50 db.**

Introduction

IT IS hardly necessary to enlarge upon the extraordinary importance of multipliers for electronic analog computation. Yet those who have worked with existing multipliers probably all agree that none of these are really satisfactory, especially with respect to long term drifts. Where nonlinear circuit elements are used,[1] one has to depend on the accuracy of their characteristic over a large range. If a pulse modulation method is used,[2] fixed dc voltages have to be added to the inputs to make them always positive. This means balancing unwanted terms in the result. The "difference of squares" method[3] requires balancing two signal branches.

Carriers have been used for analog multiplication in various instances. Chance *et al.*[1] have described a multiplier using two carriers; its inputs accept only signals of one sign, that is, the input signals cannot go through zero. R. L. Sydnor *et al.* describe in a recent paper[4] a device which uses carriers; however, the dc drift is eliminated at the expense of eliminating zero frequency

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† Bell Telephone Labs., Inc., Murray Hill, N. J.

[1] J. A. Miller *et al.*, "Wide band analog function multipler," *Electronics*, vol. 28, pp. 160–163; February, 1955. Raytheon 329 square law tube is used.

B. Chance *et al.*, "Waveforms," M.I.T. Rad. Lab. Ser., McGraw-Hill Book Co., Inc., New York, N. Y., vol. 19, pp. 670–682; 1949. A variety of multiplier types are discussed including one using two carriers.

[2] M. Lejet Lamand, "A time division multiplier," IRE Trans., vol. EC-5, pp. 26–34; March, 1956. See also (1).

[3] B. Chance *et al.*, "A quarter square multiplier using a segmented parabolic characteristic," *Rev. of Sci. Instr.*, vol. 22, pp. 683–688; September, 1951.

[4] R. L. Sydnor *et al.*, "Analog multipliers and squarers using a multigrid modulator," IRE Trans., vol. EC-5, pp. 82–85; June, 1956.

signals altogether. Due to the necessary band-pass filters, the bandwidth of the device is so narrow as to admit, in effect, only sinusoidal signals. Thus, it could hardly be used in an analog computing system. The use of a combination of amplitude modulation and frequency modulation is described by W. A. McCool.[5]

In all these cases dc amplifiers are necessary, which makes the problem of drift annoying and difficult to solve.

This paper describes a multiplier which is inherently free of drifts, since it does not make use of dc amplifiers. Yet, it is capable of handling wide band input signals, including zero frequency (dc). It is basically a "four-quadrant" device, that is, the polarity of the output is automatically correct for any combination of input polarities without recourse to such tricks as adding fixed voltages to the inputs and subtracting undesired terms in the output. Multiplication is performed in a ring modulator in such a way that distortion terms up to and including the third order are separated in frequency, and therefore, can be removed by filtering. This is achieved by impressing each of the two input signals on its own carrier (Fig. 1). The two resulting modulated carriers are then applied to the basic multiplying unit, which is not, and does not have to be, perfect. The product is centered at the frequency equal to the sum of the carrier frequencies, while distortions appear at different frequencies. Altogether four ring modulators are required, two for modulating the input signals M_1, M_2, one as basic multiplying unit, M_3, and one for demodulation of the product signal, M_4.

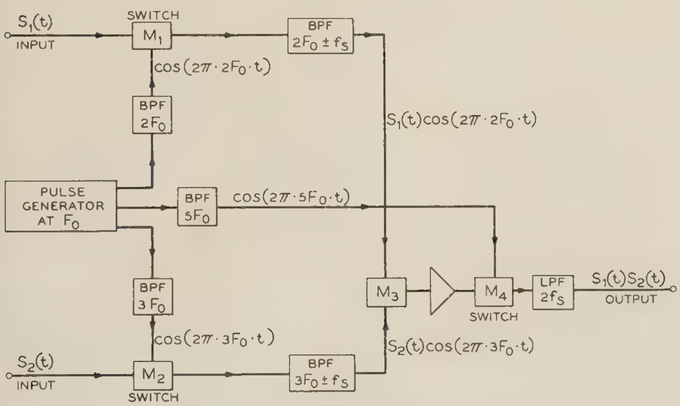

Fig. 1—Block diagram of multiplier.

Theory

Before describing the multiplier as a whole it is advisable to consider the modulators in detail. Three of them (M_1, M_2, M_4) are used as "reversing switches" (Fig. 2). The carrier is supplied through a transformer. Either the signal input or output can be dc connected, while the other is ac coupled. The carrier is always considerably larger than the signal, thus biasing alternately two varistors in the forward direction and the other two backwards. Hence, this modulator simply reverses the signal polarity at the carrier rate. The carrier amplitude has no effect on the output. The signal output equals the signal input times the square wave of the carrier frequency F. Let the signal input be $S(t)$ and the carrier $\cos(2\pi Ft)$. Hence, the output becomes

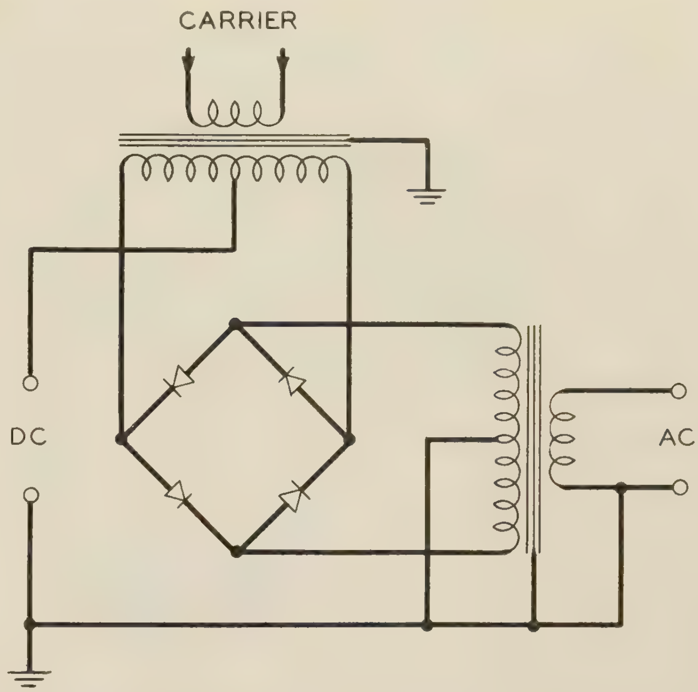

Fig. 2—Ring modulator as reversing switch.

$$S(t) \cdot \sum_{1}^{\infty} (-1)^n \frac{\cos(2\pi nFt)}{2n-1}$$

where the series represents the square wave. The carrier frequency should be much larger than the signal bandwidth, so that all, but the first term of the series can be removed by a band-pass filter. The filter output is

$$S(t) \cos(2\pi Ft).^6 \qquad (1)$$

The performance of the multiplier depends critically on the performance of these switches. Those of the experimental model have a range of 60 db, that is, the carrier leak for zero input is 60 db below the maximum signal which is handled linearly.

One of the modulators, M_3, the basic multiplying unit, is operated differently. No carrier is supplied. Instead, two signals are applied symmetrically through the transformers at low levels in order to avoid saturation of the varistors (Fig. 3). Analyzing the circuit, for the voltages across the four legs of the ring, one finds the following expressions:

[5] W. A. McCool, "An am-fm electronic analog multiplier," Proc. IRE, vol. 41, pp. 1470–1476; October, 1953.

[6] The process described is known as "double side band suppressed carrier modulation."

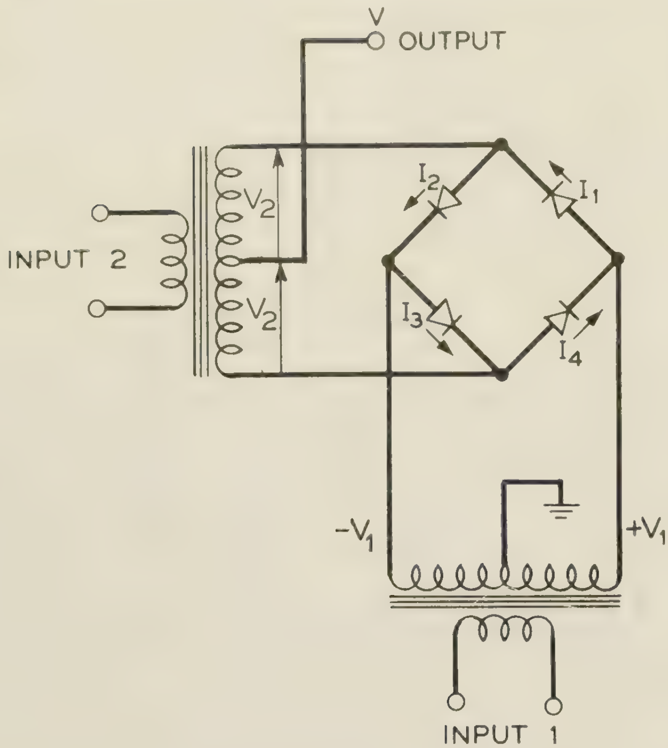

Fig. 3—Ring modulator as basic multiplying unit.

$$\begin{aligned} U_1 &= -V + V_1 - V_2 \\ U_2 &= +V + V_1 + V_2 \\ U_3 &= -V - V_1 + V_2 \\ U_4 &= +V - V_1 - V_2. \end{aligned} \tag{2}$$

The currents flowing through the four legs must satisfy the relation

$$I_1 + I_3 = I_2 + I_4. \tag{3}$$

Let us now assume that for each diode the following current voltage relation holds

$$I = GV + \alpha V^2. \tag{4}$$

Substituting into this equation I_k for I and U_k from (2) for V, one arrives at these four equations

$$\begin{aligned} I_1 &= G(-V + V_1 - V_2) + \alpha(-V + V_1 - V_2)^2, \\ I_2 &= G(+V + V_1 + V_2) + \alpha(+V + V_1 + V_2)^2, \\ I_3 &= G(-V - V_1 + V_2) + \alpha(-V - V_1 + V_2)^2. \\ I_4 &= G(+V - V_1 - V_2) + \alpha(+V - V_1 - V_2)^2. \end{aligned} \tag{5}$$

Substituting these expressions for the currents into (3), one obtains

$$V = -\frac{\alpha}{G} V_1 V_2.$$

This equation appears to say that the ring modulator is a perfect multiplier. However, in practice it has two defects. First, it cannot handle dc inputs, because of the transformers. Second, the four varistors will always differ slightly from each other. A glance at (5) shows that in this case the constants G and α vary from line to line. Hence, the result will contain—apart from the product V_1V_2—additively the following distortion terms

$$V_1,\ V_2,\ V_1^2,\ V_2^2. \tag{6}$$

Furthermore, it might be necessary to include third order terms in (4), which will give rise to still more distortion terms

$$V_1^3,\ V_1^2V_2,\ V_1V_2^2,\ V_2^3. \tag{7}$$

We proceed now to show how the arrangement of Fig. 1 eliminates both defects. The input signals $S_1(t)$ and $S_2(t)$ are assumed to contain no frequencies above f_s. They are passed through the reversing switches M_1 and M_2, respectively, the dc connections being made to the inputs. The rate of reversals is set at $2F_0$ for the first and at $3F_0$ for the second signal, F_0 being larger than $4f_s$. The choice of the carrier frequency ratio 2:3 will be explained later. After passing the outputs of the switches through filters of bandwidth $2f_s$, which are centered at $2F_0$ and $3F_0$ respectively, the following signals are obtained

$$V_1 = S_1(t) \cos (2\pi 2F_0 t) \quad V_2 = S_2(t) \cos (2\pi 3F_0 t).$$

V_1 and V_2 are now combined in the basic multiplier, M_3, whose output is the product plus distortion terms. Only the product V_1V_2 is desired. It has two components, one in a frequency band centered at F_0, the other one centered at $5F_0$ (sum and difference of the two carrier frequencies $2F_0$, $3F_0$). All distortion terms up to and including the third order, that is, the terms listed explicitly above (6) and (7), fall into frequency bands which do not coincide with $5F_0$. Hence, a band-pass filter centered at $5F_0$ will eliminate these distortions. The component picked out at $5F_0$ is simply

$$S_1(t)S_2(t) \cos (2\pi 5F_0 t). \tag{8}$$

Although higher than third order distortion terms are too small to cause any difficulty, we shall consider them briefly. Unfortunately, no choice of carrier frequencies will prevent two of the five fourth-order terms from having components at the frequency F_1+F_2, namely $V_1V_2^3$ and $V_2V_1^3$. However, each of these terms splits into eight components at different frequencies, of which only two fall on F_1+F_2. Since fourth order terms are small to begin with, their contribution to the component F_1+F_2 will be negligible. This is borne out in practice.

Eq. (8) shows that M_3 has, in fact, achieved the multiplication. The result is still impressed on a carrier. This is, however, an advantage, since the signal is of very low level and has to be amplified. No dc amplifier is required. The final demodulation is performed in M_4, which is run as a reversing switch with cos $(2\pi 5F_0 t)$ as

carrier, the dc connection being made to the output.[7] This switch will change the sign of its input (8) whenever $\cos(2\pi 5F_0t)$ is negative. Hence, its output will be

$$S_1(t)S_2(t)\,|\cos(2\pi 5F_0t)|,$$

or

$$S_1(t)S_2(t)\left(\frac{2}{\pi} - \sum_1^\infty \frac{(-)^n}{\pi(n^2-1/4)} \cos(2\pi n 10F_0t)\right). \qquad (9)$$

The process is shown in Fig. 4, (a) showing the wave form (8), (b) the carrier, and (c) the wave form (9). A low-pass filter removes that part of the signal which is represented by the series (high frequency) and produces an output proportional to

$$S_1(t)S_2(t).$$

The switch can handle voltages up to a few volts, so that no further amplification is necessary.

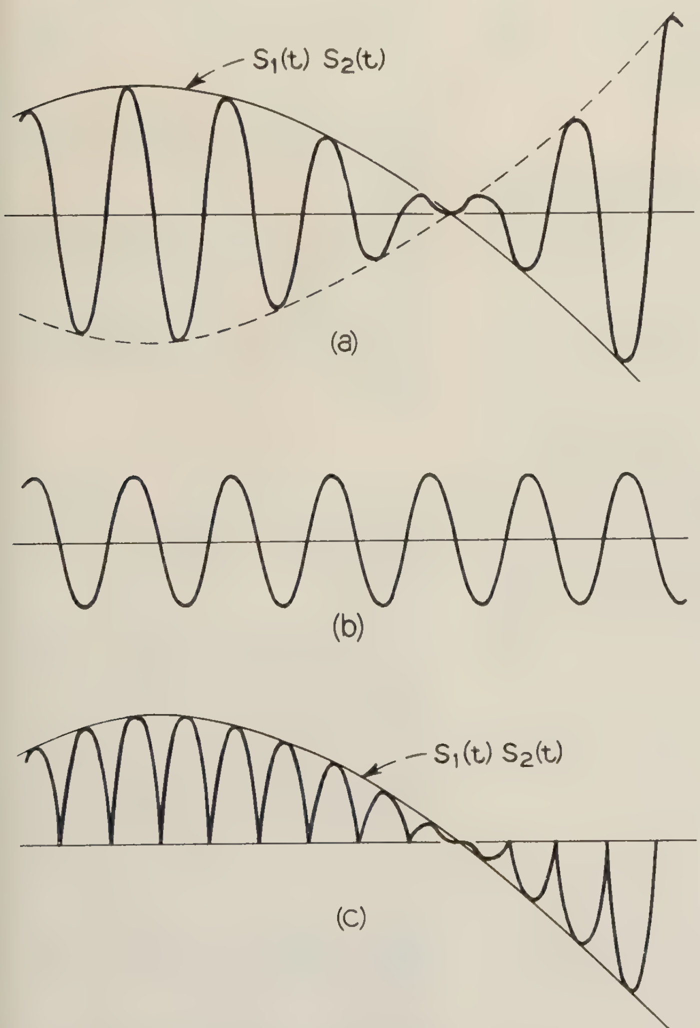

Fig. 4—Waveforms associated with switch M_4.

[7] A rectifier and envelope detector would give only the absolute value of the product, since the envelope of (8) is evidently $|S_1S_2|$.

It is important that the phase of the demodulating carrier remains fixed with respect to the phases of the other two. This is why all three carriers are derived from the same oscillator.

It is now easy to see that the band-pass filter centered at $5F_0$ can be omitted, since the demodulation and low-pass filtering performs this function; it was introduced above to facilitate the explanation.

There is nothing mystical about the ratio 2:3 of the carrier frequencies. It provides the lowest possible frequency of the product carrier for a separation of the distortion terms in frequency. Let the two input carrier frequencies be F_1, F_2 and the product carrier frequency F_1+F_2. The various terms $V_1^m V_2^n$ occupy the following frequencies

$$F = |pF_1 + qF_2| \qquad p, q \text{ integers.}$$

F_1F_2 can be expressed with any desired accuracy as

$$F_1 = \mu F_0$$
$$F_2 = \nu F_0$$

where μ and ν are integers which have no common divisor. Hence

$$F = |p\mu + q\nu|\,F_0.$$

An elementary result of number theory states that $p\mu+q\nu$ assumes any integral value as p and q vary. Hence, the frequencies F are spaced F_0 apart. To obtain the smallest product carrier frequency $F_1+F_2=(\mu+\nu)F_0$ one chooses the smallest integers μ, ν, for which the system works. For 1, 1 or 1, 2 it evidently does not, but it works for 2, 3.

Reduction to Practice

A multiplier has been built according to these principles. It has been tested and found to fulfill all expectations. The following are its characteristics according to measurements.

$F_0=45$ kc. The reversing switches, therefore, run at the following carrier frequencies: 90 kc, 135 kc, and 225 kc, respectively.

If x and y are the two inputs measured in volts, the output is

$$Z = \frac{x,\ y}{50} \text{ volts.}$$

The inputs are at 600 ohms, 7 volts maximum from dc to 7 kc, the output is at 100 ohms from dc to 14 kc, 1 volt maximum.

Errors are $\pm$(1 per cent of the output $+0.05$ per cent of the larger input).

For $x=7$, $y=0$, the residual output is $z=0.0015$ v rms

The output is free of drifts.

The photograph of Fig. 5 shows the output of the multiplier for a sine wave and a triangular wave as inputs. A picture like this provides a simple test for

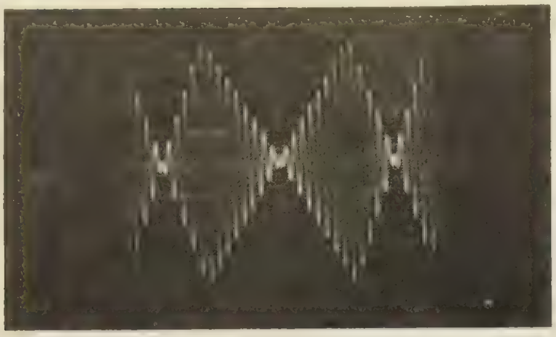

Fig. 5—Oscilloscope trace showing the product of a sinewave and a triangular wave.

linearity with respect to one input since the envelope of the trace has to be the original triangular wave and its reflection at the time axis. Note that this envelope consists of perfectly straight lines.

This multiplier should prove to be very useful where a fast response is required and where even slight drifts are not tolerable.

ACKNOWLEDGMENT

The author is indebted to A. J. Prestigiacomo for building this multiplier according to the principles described above.

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Picard's Method and Analog Computation*

Picard's method of solving differential equations has often been taken into consideration when explaining the role of direct feedback in analog computers. To present our point of view, we shall take the following differential equation

$$\frac{dy}{dt} = f(y, t)\, y(0) = a$$

and the equivalent computing circuit (Fig. 1). It is easily understood that the generality of the discussion is in no way restricted by the type of the equation taken.

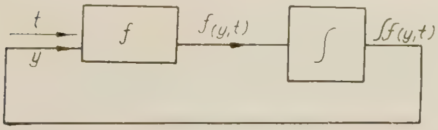

Fig. 1

In order to establish the relation between the method of successive approximations and analog computation, a mathematical procedure will be proposed, which differs somewhat from the one usually applied, but which is based on the same theoretical foundations.

As is known, the solution of a differential equation by Picard's method, requires a series of successive integrations of the form

$$y_{m+1} = a + \int_0^t f(y_m, t)dt \quad m = 0, 1, \cdots$$

to be carried out. Although very general, the method has severe practical limitations, since the calculations involved are usually difficult and time-consuming.

Our aim is to investigate the possibility of a modified iterative procedure, where, in principle, the error

$$\epsilon(m) = y_m - y$$

is a continuous, decreasing function of time

$$\epsilon = v(t).$$

In addition

$$\epsilon \to 0$$

when

$$t \to 0$$

meaning that the error should be reduced to minimum in a negligible fraction of the interval of integration.

For this purpose, the following series of approximating functions

$$y(0) + \int_0^t f(y_0, t)\, dt,\ y_1(t_1) + \int_{t_1}^t f(y_1, t)\, dt, \cdots,$$
$$y_n(t_n) + \int_{t_m}^t f(y_m, t)dt$$

is taken. The lower limits of integration, t_m, correspond to the instants of replacing y_{m-1} by y_m. Let us assume that this replacing is instantaneous, which, in practice, can be achieved by use of electronic switching. If the independent variable, t, is represented by time, the process of error reducing is also time dependent, and looks as shown in Fig. 2. Besides, there are no obstacles to letting

$$t_m - t_{m-1} \to 0.$$

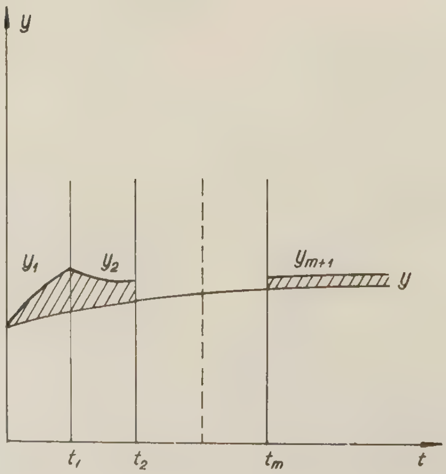

Fig. 2

As a result, smaller and smaller portions of each curve

$$y_m$$

are taken into consideration, while, at the same time, their number grows. In the limiting case, the family of all y_m will belong to a continuous set.

From the point of view of realization, it is easily seen that such a procedure requires:

1) that integrations be performed in real time,

2) that integrals be obtained by means of the transfer functions of computing circuits, or by any other process which ensures the calculation of

$$\int f(y, t)dt$$

under the same conditions for a whole class of operators f.

3) In the limiting case, direct feedback can be considered as replacing instantaneously y_{m-1} by y_m.

The above approach may help in bringing closer together certain analytical methods and the principles of analog computation. Besides other advantages, such a treatment can be used to show that all problems solvable by Picard's method can be, in principle, solved on analog computers.

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* Received by the PGEC, April 5, 1956; revised manuscript received October 4, 1956.

Extending the Operational Time of Analog Integrators*

There are two principal factors which limit the length of time for which an analog integrator (such as the customary RC opera-

* Received by the PGEC, August 1, 1956; revised manuscript received December 10, 1956.

tional integrator, can operate. The first, and most familiar of these, is "drift," and is inherent in the operation of the device. Both a larger integrator time constant and a higher amplifier gain will reduce this drift. A second cause, which can become serious if the input is consistently of one polarity (as it often is in certain control applications) is amplifier saturation. Eventually, the amplifier reaches its maximum output voltage and can go no higher. While a larger time constant will allow a longer integration time when saturation is a limiting factor, increasing the amplifier gain will have no effect. Attenuating the input also increases the integrating time. However, if the integrating time is to be increased by a large number (a factor of several hundred to a thousand) attenuating the input will usually decrease the signal-to-noise ratio by an unbearable amount when the noise is produced in the integrator, and the physical size of the components necessary for a suitable time constant becomes impractical. For example, if an integrator has a capacitor whose value is 10 microfarads and as large a resistor as can be used, a capacitor of 5000 microfarads is necessary if the integrating time is to be increased by a factor of 500. When this capacitor must also be a precision capacitor (as is always the case), such a procedure is out of the question.

It is possible to duplicate the effect of such a large capacitor, however, by storing the value of the integral on an electronic counter in addition to the actual capacitor itself, and thus increase the integrating time by a factor as large as 1000 without introducing excessive error. This procedure, as outlined below, will not affect the drift, only the saturation.

Fig. 1 illustrates the device's principles. It

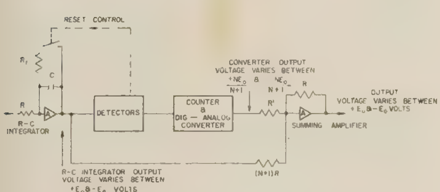

Fig. 1—Integrator connections to provide correctly-weighted output

is assumed that the maximum and minimum voltages in the amplifier's linear range are $+E_0$ and $-E_0$ volts. The detectors determine when the integrator output reaches an extreme and either increase or decrease the state of a reversible electronic counter by one unit. The detectors also discharge the capacitor through the resistance Rr (which may be only the inherent resistance of an electronic switch). The counter state is transformed into a voltage by means of a digital-to-analog converter, and the voltage is added to the integrator output with a suitable scale factor. The counter has $2N+1$ states, and counts from $-N$ through zero to $+N$. A separate summing amplifier is not always necessary, since in many computers this amplifier would merely be the computing amplifier for the next level of computation. The over-all effect is that of a simple integrator with a time constant equal to NRC, although for computing drift only a time constant of RC should be used.

The principal sources of error are due to the integrating time lost while the capacitor is being reset, errors in the detectors, and errors in the digital-to-analog converter. None of these errors increase with time, and in this sense they are not systematic. If "state-of-the-art" devices are used, the additional error contributed by this extra circuitry can be held below one per cent. That is, if the integrator by itself has an accuracy of two per cent, it would have an accuracy of about three per cent with the additional features. Such a small error can only be maintained up to values of N of about 1000. Above this, errors in the digital-to-analog converter may become excessive.

The scheme described here requires considerably more complexity than a simple integrator. However, the additional circuitry will often be smaller, lighter, and more accurate than resistors and capacitors large enough to produce a corresponding effect.

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An Integral-Error-Squared Method for Evaluating Analog Computer Components*

In order to obtain a single number by which to evaluate components or systems, an integral-error-squared system may be set up on the usual analog computer installation. The circuit shown in Fig. 1 contains a servomultiplier which is undergoing such an error test. An input voltage X drives the potentiometer sliders and serves as the independent variable for the 30×30-inch plotter, shown at the bottom of the figure. With S_1 closed, S_2 in the position shown, and all other switches open, the output from the amplifier proceeding the squarer is 10 times the error present in the servomechanism itself. To check the multiplying potentiometers, switches S_3 to S_7 may be closed as required.

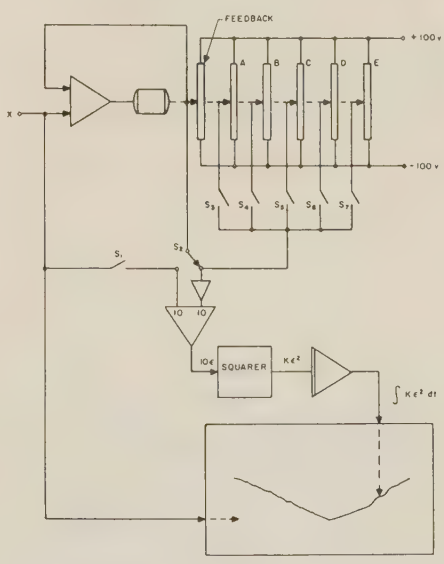

Fig. 1—Circuit for integral-error-squared plot.

* Received by the PGEC, May 1, 1956; revised manuscript received November 2, 1956. This paper presents one phase of research carried out at the Jet Propulsion Lab., Calif. Inst. of Tech. under Contract No. DA-04-495-Ord 18, sponsored by the Dept. of the Army, Ordnance Corps.

The most crucial component of this measuring system is the squaring device. A diode function generator[1] was used for this purpose. To generate the required parabolic function, a multitonic setup may be used or monotonic diode function generators may be placed in the feedback loop of operational amplifiers. It is not as important that the parabolic function be generated exactly as it is that the function be well balanced in respect to positive and negative inputs. The diode function generator was chosen for this application because of its high speed of response in respect to the component under test and for its ability to generate steep slopes under the proper setup conditions.

The output of the squarer goes directly into a conventional integrator with a 1-megohm input resistor and a 1-microfarad feedback condenser. The Y axis of the recorder receives the output of the integrator and thus produces a trace which represents the integral-error-squared response of the error of the servomultiplier. Standard times are necessary to make comparisons of plots. For example, in the work done with servomultipliers, runs were made at the rate of 10 volts per second.

An example of the results of an integral-error-squared test is shown in Fig. 2. The

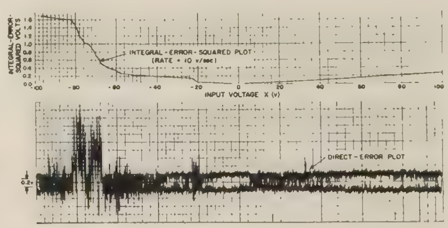

Fig. 2—Comparison of direct-error and integral-error-squared methods.

upper curve represents the trace obtained from the circuit of Fig. 1 for a particular multiplying potentiometer which happened to be noisy. The lower curve is a direct-error plot of the same servomultiplier arrangement. In this case, the Y axis of the recorder is driven directly by the voltage representing 10 times the error.

It will be noted that where large noise peaks occur on the direct-error plot, steep slopes appear on the integral-error-squared curve.

The final readings at plus- and minus-100-volts input are the figures used for evaluating the particular servomultiplier under test.

[1] R. Bruns, "An improved diode function generator for analog computers," *Proc. Natl. Simulation Conference*, pp. 32.1–32.7; January, 1956.

Other advantages[2] in the integral-error-squared method are the speed with which a complete run can be made and the proper utilization of the recorder which may have a more limited frequency response than the servomultiplier under test.

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[2] R. Bruns, "Servomultiplier error study," *Proc. of Association for Computing Machinery*, UCLA, Los Angeles, Calif., August, 1956.

A Note on the Accuracy of Differential Analyzers*

The limitations on the accuracy of electronic differential analyzers solving linear differential equations were investigated by MacNee.[1] In the case of the harmonic equation, *e.g.*, he found that component phase shifts yield an exponential buildup or decay of the oscillation.

The purpose of this note is to show that in the case of a differential analyzer solution of an oscillating relay servo, the same component phase shifts yield an incorrect amplitude and frequency of the oscillation. A rough quantitative theory utilizing the concept of the describing function[2] is presented to illustrate how the computer errors may be predicted. Finally the importance of a suitable choice of the computing time in repetitive analog computers is illustrated by an example.

The system under investigation is supposed to contain only one relay and may be represented as a single loop such as shown in Fig. 1. The Barkhausen criterion for steady oscillations in such a loop requires a total loop phase shift of $\phi=0°$, at unity loop gain.

In the case considered the phase conditions determine the frequency of the oscillation. On the other hand the amplitude adjusts itself to such a value as to assure unity loop gain.

Fig. 1—Functional diagram of a servomechanism containing a single relay.

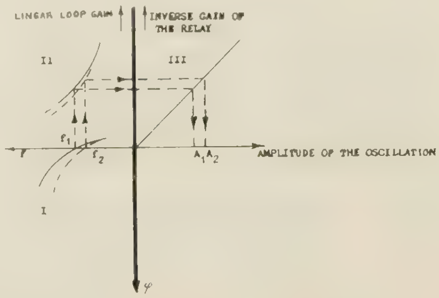

Fig. 2—Error determining mechanism of the electronic analog of a relay-servo.

The way this happens is illustrated for both the real system and the electronic analog in Fig. 2. A possible phase-shift vs frequency characteristics of the system investigated (full trace) and of the electronic analog (dashed line) are given in the quadrant denoted by I. The true frequency of the solution (f_1) and the one actually obtained (f_2) are given by the intersection of these curves with the $\phi=0°$ line. The linear loop gain corresponding to f_1 and f_2 may be obtained from the respective frequency response curves given in quadrant II. Finally, in quadrant III the inverse gain of the relay is represented as a function of the amplitude of the oscillation following the already mentioned investigations of Kochenburger. (The relay here is supposed to have negligible backlash.)

The true and the actually computed amplitude of the oscillation A_1 and A_2 respectively, are thus easily determined by following the arrow (Fig. 2) and having the Barkhausen criterion in mind.

In systems where the loop gain is a high order function of the frequency, a small phase shift error may yield a large error in the amplitude of the solution. There is no increase or decrease of this amplitude as experienced in the case of the harmonic equation.

As a practical example, a relay type servomechanism was analyzed, described by the following equations:

$$0.2\, y'' + y' = 16\, x$$

$$0.2\, x'' + x' = 20 \text{ sign } \epsilon$$

$$\epsilon = y + 0.9\, y'$$

where x and y denote angular displacements. ϵ denotes the error voltage which actuates the relay. The relay output is denoted by sgn ϵ (sign of ϵ).

The high frequency time constant of the adder and integrator of the repetitive computer employed was $T=5\ \mu$s, the operational amplifier had a gain of 1500 and at first a working time $t_1=4\ \mu$s was chosen. An additional requirement was that at least five full periods of the oscillation should occur within t_1. An error of 90 per cent resulted in the amplitude y of the solution in comparison with results obtained by a numerical analysis by the Kochenburger method. The same computer however was able to solve the problem with an accuracy better than 10 per cent by a suitable choice of the working times.[3]

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* Received by the PGEC, August 2, 1956; revised manuscript received December 20, 1956.

[1] A. B. MacNee, "Some limitations on the accuracy of differential analyzers," Proc. IRE, vol. 40, pp. 303–308; March, 1952.

[2] R. J. Kochenburger, "A frequency response method for analyzing and synthesizing contactor servomechanisms," *Trans. AIEE*, vol. 69, pp. 270–284; 1950.

[3] A. Fuchs: "Working time in repetitive analog computers," IRE Trans., vol. EC-5, p. 94; June, 1956.

Ways of Developing Soviet Computer Production*

Very little has been published in the United States about Soviet Computers. For this reason we are printing this rather lengthy series of abstracts of computer papers given at a conference in Moscow on March 12–17, 1956.

The complete papers were not available, so that it is difficult to learn of technical innovations. Also, without the context, the meaning is not always clear, and the abstracts unavoidably suffered in translation. One does gain an impression of the wide range of activities taking place in the U.S.S.R., and these should be of interest to many readers.

We are indebted to Prof. Alwin Walther of the Institut für Praktische Mathematik, Technische Hochschule, Darmstadt, Germany, for providing the abstracts and to the IBM Research Laboratory, Poughkeepsie, N. Y., for making this translation available. The translation was prepared by G. O. Tarnawsky of the IBM Research Laboratory with the assistance of the Research Library Staff—*Editor*

A. Universal Digital Computers

Chairman—Academician S. A. Lebedev

I. Alexandridi, T. M.—Engineer

Electrostatic Memory of M-2 Computer

1. *General Principles of The Memory Operation:* Information in the electrostatic memory is stored in the form of a certain distribution of static electric charges on the screen of a cathode-ray tube of the 13 LO-37 type.

A zero is represented by a dot while a one is presented by a dash. The dash is used in reading, the signals being taken from the screen of the cathode-ray tube with a fine metallic screen.

2. *Block-Diagram:* Memory of the parallel access type consists of 512 words of 34 bits each.

In operation, the selection of an address on the cathode-ray tube is controlled by the program counter through circuits which set the deflection voltages and provide the signals to turn the beam on.

3. *Selection of Tubes:* A special stand is constructed for the selection of tubes, in which the tubes are thoroughly checked for the maximum permissible number of read-around cycles. Tubes which can operate at a read-around ratio of more than 800 cycles are considered suitable. The maximum possible read-around ratio in the machine is 170. The service life of the tubes is not less than a year. Some reasons for rejection of tubes out of the lot were burnt-out filament and, in two of the cases, increased noise.

II. Dashevskii, L. N.—Candidate Technical Sciences

Performance of Small Electronic Calculator Academy of Sciences, Ukrainian, S.S.R.

1. The small electronic calculator (MESM), built in Kiev under the supervision of Academician S. A. Lebedev in 1951, has been in operation since 1952. By December 1, 1955, the machine had operated for over 13,000 hours. It was used to solve several practical problems as well as to instruct the personnel operating and programming it.

2. The machine solved problems mainly related to the integration of linear and nonlinear differential equations, the determination of limits in the sphere of the stability of dynamic systems expressed by equations to the tenth power of the Routh, Hurwitz, Neimark, etc., methods.

3. The main technological data of the machine are:

a) Rate—50 operations per second;
b) Number of bits—20, point being fixed before the highest order bit;
c) Operational memory—active: 31 numbers and 40 commands; passive: 31 numbers and 63 commands;
d) External memory—about 2000 words on a magnetic drum;
e) Number of tubes—7200 (after the vacuum diodes are replaced by germanium diodes, the number will be reduced to 3000);
f) Results displayed at the rate of one number per second with the aid of a number printing mechanism.

4. A regular check is being kept on the machine of the operating conditions of the tubes, and reasons for their discard. It has been established that the lifetime of a tube of the type 6N8S, 6N9S, or 6X6S is somewhere between 8000 and 9000 hours.

5. A sequence of heating of the tubes is used in the machine (in groups of 6–10); checks were made on the performance of the tubes in this type of operation.

III. Kartsev, M. A.—Engineer

Arithmetical Unit of M-2 Computer

1. *General Characteristic of the Arithmetical Unit:* The arithmetical unit of M-2 is a parallel type, made up of 4 static trigger registers of 34 bits, operating at a frequency of 80 kc. The mechanism is intended for operation utilizing either fixed-point or floating-point numbers.

2. *Circuit Elements:* The triggers used in connection with 6N8S double triodes as well as the external bias and input to networks are connected through copper-oxide rectifiers.

All logical circuits ("and," "or," "non-coincidence") employ diodes, in connection with which copper-oxide rectifiers (KVMP-2-7) are used.

The final pulsing is done by flip-flops, utilizing 6N8S double triodes. Because the triodes in the flip-flops are connected in series, the characteristics of these flip-flops are almost identical with the pentode multivibrator; at the same time the scatter of the triode flip-flop characteristics is narrower and the lifetime is longer than for the pentode multivibrator.

1:1 pulse transformers are used for altering the polarity of the pulses.

In all, the arithmetical unit employs 12 tubes to one bit, the tubes all being of the 6N8S type.

3. *Execution of Operation with Numbers:* Addition, with a fixed point, is executed in two steps: the formation of units using binary carry and displaying the sum. The first step can be separated from the second, which is convenient in division and comparison of figures.

Subtraction is executed as an addition of the complement; multiplication as a series of additions and shifts; division as a series of subtractions and shifts.

In addition and subtraction with a floating point the characteristic appears first; multiplication and division with floating point consist of additions (subtractions) of the characteristics and multiplication (division) of the mantissas. All the operations with the floating point terminate by normalizing the result.

4. *Some Data on Operation:* One of the maintenance methods consists of performing the shift operations and introducing the control problems after the heater voltage is decreased from 6.3 v to 4.7 v.

A reliability check of the tubes is done every 1500 hours. Tubes are checked in advance.

IV. Mel'nikov, V. A.—Engineer

Some Questions on Technological Performance of the Large Electronic Computer BESM of Academy of Sciences of U.S.S.R.

The reliability and dependability of performance of electronic calculating machines qualitatively characterizes the operation of computers, and therefore, the basic problem of technological performance is the determination of such methods and means which would assure the uninterrupted performance of the machine for the period of calculation.

The possibility of obtaining uninterrupted operation of the machine is attainable with special reliability preparation.

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The combination of methods of reliability control and test programs will assure the uncovering of elements having little dependability and this will considerably increase the reliability and dependability of the machine's performance.

The statistical material, gathered on the basis of performance of the machine during 1952–1955, permits giving definite recommendations essential for planning and operation of universal high-speed electronic computers.

V. Miamlin, A. N.—Engineer

Test of Technological Performance of the "Arrow-1" (Strela-1) Computer and its Modernization

1. *Technological Characteristics and Construction of Computer:* "Arrow-1" is a triple address universal machine of parallel operation, employing floating point.

The range of numbers is from 10^{-19} to 10^{+19} with nine significant figures.

Speed is 3000 operations per second.

The machine is composed of memory mechanisms consisting of cathode-ray tubes, magnetic tapes and diodes, arithmetical unit, and mechanical devices for input and output.

The separate units of the machine are made in the form of from 2 to 9 tubes per cell. It would be more convenient to operate these units by single cells.

The circuits of the machine are unnecessarily bulky and complex.

2. *Modernization:* The modernization was conducted with the aim of increasing the dependability and speed of operation.

The plans of the central controls, the arithmetical unit and controls of the memory magnetic tape were subjected to change.

The types of reliability control introduced to all machine units guarantee correct operation of the system in the course of a week. The exception to this is the operating memory device.

The work carried out made it possible to raise the time of the correct operation of the machine from 10 or 11 hours a day in January–February, 1955, to 19 to 20 hours in January–February, 1956, and to raise the speed from 2000 to 3000 operations per second.

3. *Type of Operation and Indicators of the Machine's Performance:* The machine is being checked for reliability once a week in the course of 16 to 24 hours. Control of accuracy of performance of the memory device was conducted daily.

The comparative analysis of the machine's operation for January–February, 1955, and for January-February, 1956, allows for an evaluation of the extent to which the dependability of the performance of the machine has increased.

4. *Conclusions:* "Arrow-1" computer has a compact well-planned system of commands, convenient for programming. Possibility of carrying out arithmetical and logical operations by groups, in most cases, reduces the time for solution of problems.

A successful improvement in the computer appears to be the inclusion of memory devices which utilize diodes and which are used to store constants and standard subprograms, and the use of punched cards for input and output.

At the same time one cannot consider as successful and constructive the following:

a) The use of a wide magnetic tape;
b) The absence of a sufficiently high-speed buffer memory device;
c) The construction of the units of the machine in 9-tube cells;
d) The bringing out of a large number of circuit components on the back panel.

For the necessary technological operation of the machine, the performance coefficient is about 65 to 70 per cent.

VI. Neslukhovskii, K. S.—Engineer

Comparison of Parallel and Series Type Universal Computers With and Without Sequential Orders

The differences in the basic layout of machines with and without sequential orders are examined.

Machines with and without sequential orders are compared from the point of view of the number of mechanisms functioning.

Time used for the completion of operation in machines with and without sequential orders is determined.

And, finally, machines of the types mentioned are compared from the point of view of speed of operation.

VII. Pogrebinskii, S. B.—Engineer

Mechanism for Transforming Codes From One System of Coding Into Another

1. The conversion from one system of coding to another in large binary computers (utilizing binary coding BVM) is usually brought about with the aid of programs. There are ways of developing types of programs which would speed up the process of conversion.

2. The program of straight conversion leads to a subtraction according to Horner's system of the polynomial, representing the number in the decimal system of notation, and demands the production of 40 to 60 operations. The reverse conversion is performed by a known algorithm and the development takes nearly the same number of operations.

3. The proposed method of computation of the polynomial uses the assembly of binary-coded decimals, distribted in a predetermined manner, which allows for the computing to be done in one operation, equivalent to multiplication. The $(i+1)$st term of the polynomial N can be obtained from the ith term by shifting the sum obtained earlier and adding the binary-coded decimal, if the $(i+1)$st coefficient of the binary representation of the number being converted is one. An analogous method is also proposed for the reverse conversion.

4. In the operation of the multiplication device of the BVM the number of additional units for a straight conversion is 5 to 6 diodes for each decimal place of the number introduced; for the reverse conversion, two units for each decimal place.

5. The time for conversion is equal to the time of one multiplication. A direct conversion can usually be combined in time with the introduction of original data into the machine.

6. The device for direct and reverse conversion working according to the method described, is used in the layouts of the specialized machine. The static mechanism of the reverse conversion is included in the layout of Small Electronic Calculator (MESM) of the Academy of Sciences, Ukranian, S.S.R.

VIII. Rameev, B. I.—Engineer

Universal Automatic Digital Computer of "Ural" Type

1. *Introduction:* Area of application, problem solving, basic needs in construction of machine.

2. *Basic Parameters of Machine:* Operational and technological indicators.

Time for solution of some problems.

3. *System of Orders:* Features of the system of orders.

4. *Brief Description of Machine:* Composition of machine. Basic parameters and features of layout and construction of separate devices.

5. *Construction of Machine:* Features of construction of separate arrangements of units, as well as of the machine as a whole. Assembly.

6. *Conclusion:* Comparison of "Ural" machine with famous serial machines of this class.

IX. Shcherbakov, O. K.—Engineeer

Questions of Power-Supply Principles of Electronic Computers

Although the problems that arise in connection with power supplies are of great and immediate importance in design and operation of digital computers, there is very little literature on the subject.

Features of ac and dc power supplies of electronic computers are being analyzed.

Construction principles of shielding, indication and signalization are examined.

Test was performed on power supplies of the large electronic computer (BESM) of the Academy of Sciences of U.S.S.R., on one basis of which some recommendations are given for the construction of power supplies for electronic digital computers which are simple, dependable, and have a long life.

X. Alekseev, V. IA.—Engineer

Technological Characteristics of Dynamic Flip-Flops

1. The principle of the dynamic trigger system utilizing a triode with a memory capacity and its superiority over the usual flip-flop system with voltage connections is examined.

2. Technological characteristics of the dynamic flip-flops with memory capacity employing the 6N3P double triode (load, frequency, amplitude) are shown. Power-supply requirements are examined.

3. Two types of circuits for a dynamic pentode flip-flop used as a memory device and controlling two networks are examined.

4. Technological characteristics of dynamic flip-flops with memory capacity employing the 6Z2P pentode (load, frequency, amplitude) are demonstrated. Power-supply requirements are examined.

XI. Bardizh, V. V.—Candidate Technical Sciences, Vizuniu, I.—Engineer, and Kobelev, V. V.—Engineer

Magnetic Memory with Decoders Employing Tape Magnetic Cores

1. Application of ferrite cores to memory mechanisms of high-speed calculating machines appears to be quite promising.

2. One of the methods of raising the dependability of performance of the memory mechanism is to raise the ratio of the two currents, acting on the selected and nonselected cores. Application of dynamic displacement permits making this ratio 3 to 1 quite easily without introducing any noise into the output signals.

3. Limitation of number of cores on a sense winding, together with the application of matrices containing these windings, substantially increases the signal-to-noise ratio.

4. Application of magnetic decoders, employing cores of tape materials, in the memory matrix, improves the dependability of performance of the mechanism because of high-temperature-stability characteristics of magnetic-tape materials.

XII. Golovistikov, P. P.—Engineer

Circuits Based on Dynamic Flip-Flops

1. Calculating and controlling circuits of high-speed electronic machines in relation to the character of the connection existing between the logical elements, can be broken down into three types:

a) Circuits with voltage linkage between elements;
b) Circuits with pulse linkage between elements;
c) Circuits with mixed linkage between elements.

2. Circuits with pulse linkages between elements in comparison with others have the following advantages:

a) Ease of matching output resistance of the memory cell with input resistance of the diode logical circuits;
b) High operating speed with a small number of electronic tubes and other components;
c) Higher dependability, *i.e.*, the circuits work on the principle of a high gain amplifier;
d) Higher efficiency;
e) Smaller over-all dimensions (the individual elements in the circuits are operated less intensively and therefore can be of smaller size);
f) Easier replacement of tubes in the circuits with transistors;
g) Simplicity, flexibility, and universality of circuits.

3. The circuits designed with dynamic flip-flops capable of storing permitted the elimination of the basic inadequacies of the circuits used previously, namely, the necessity of input signals being in phase.

4. Circuits using dynamic flip-flops that are capable of storing can be widely used in parallel computers.

XIII. Dobrosmyslov, V. I.—Engineer

High-Speed Printer for Computers

Modern computers demand high-speed output devices. The printer, which has a continuously rotating type wheel and hammers contacting the necessary symbol as determined by the release of an electromagnet, can operate dependably at sufficiently high speeds.

At present, in the NII computer factory, there is in operation a model of such a printer. According to preliminary laboratory tests, the model assures a printing speed of from 10 to 15 lines per second.

For arriving at high printing speeds, another type of printer is being worked upon which utilizes a continuously rotating printing drum and in which the kinematics of the link between the hammer and the electromagnet have been changed.

Efficiency of the printer is determined by the number of lines which can be printed per second.

At the same time conditions must be maintained for inking the characters. Spacing of the characters on the vertical should not exceed the given limit (usually 0.15 to ± 0.3 mm). The speed of the printing arrangement is limited by the maximum speed of revolution of the printing drum.

This report will give the results of laboratory tests, and recommendations will also be given for the design of printers with a continuously rotating printing drum.

XIV. Zimarev, A. N.—Engineer, Zeidenberg, V. K.—Engineer, Lander, E. P.—Engineer, and Senatorov, Y. U. I.—Engineer

The Arithmetical Unit of an Automatic Computer of Parallel Operation Utilizing Germanium Point-Contact Transistors

1. In the design of the arithmetical unit (AU), the dynamic principle of operation of the circuit elements was selected. The advantages of this principle are shown in systems of germanium triodes.

2. Separate elements of the AU are examined: dynamic flip-flop, staging of synchronization, amplifier, flip-flop circuits.

3. The general block diagram of the arithmetical unit and results of the experiments performed on a model of such a unit are given.

XV. Zimin, V. A.—Candidate Technical Sciences

Reliability of Tubes in an Electronic Computer

1. The tubes are used in electronic computers in connection with high-speed switches.

2. Making the average tube parameters more exact has made the work in design and operation of the electronic equipment easier, and created the basis for increasing the reliability of performance of the tubes.

3. During the life term of the tube the average value of the plate current of the tube decreases. At first the current decreases rather quickly, and then it begins to increase asymptotically to 0.6 of the nominal value. At the same time there is a fluctuation in the value of the plate current equal to about 0.15 from the nominal value. Therefore, it is expedient to construct electronic circuits based on the value of plate current equal to 0.5 of the nominal value.

4. The basic defects of the tubes are found during the first few hours of operation. When the tubes are being operated at allowable load the occurrence of any defects in them drops rather quickly. After that, tube elimination begins to assume a systematic character. Therefore, technically and economically, it is expedient to stabilize the parameters of the tubes by way of corresponding tests before their insertion for use.

5. The families of static pulse characteristics of tubes permit selection of the operating load of the tubes, combining the maximum output with the longest period of operation.

6. The electronic tubes of the types 6Z4, 6P9, 6P3S, and 6N8S used in the Large Electronic Calculator (BESM) have an average service life of about 15,000 hours. The life span of the tubes depends little on the current, and is determined by criteria used for determining the unsuitability of the tubes.

XVI. Zimin, V. A.—Candidate Technical Sciences

Logical Circuits Based on Pulse Transformers and Semiconductors Diodes

1. The logical circuits, "and," "or," and "not" can be built using transformers and semiconductor diodes. If the pulse transformer has the properties of an oscillating circuit, then the force which is needed to maintain the form of the pulse decreases abruptly.

2. The dependability of point contact germanium diodes of the DGC type, during operation in electric circuits used in connection with pulse transformers, is sufficiently large.

3. The examination of the resonance properties of pulse transformers, used in connection with ferrite cores, resulted in discovery of a series of physical regularities which can be used in practice in the composition of logical circuits.

4. The study of the behavior of logical circuits utilizing pulse transformers and germanium diodes permitted the use of reverse current of the transition state of the diode for lowering of noise in the matching circuits.

5. The energy relationship in diode-transformer circuits are such that the elements operate one into the other with a transmission coefficient of about unity.

6. The system "and" and "not" were developed which do not need the application of power sources for their operation.

7. The examination of the adder based on diode-transformer elements showed the possibility of developing highly efficient circuits in the computer field.

XVII. Zubrilin, N. P.—Engineer

High-Speed Photoprinting Device (FPU)

1. High-speed output devices increase the general productivity of electronic digital computers.

2. The FPU is designed for high-speed recording from a magnetic tape to a photo-film of the results of calculations received from the BESM. The speed of recording on the photo-film is 200 decimal figures per second. In case of need the speed can be

increased considerably. The FPU can operate directly with the BESM, without intermediate recording on a magnetic tape or drum.

3. Recording on the photo-film is done with the aid of special argon-mercury tubes. The tubes are covered with number stencils which are projected on the photo-film by individual lenses. An optico-mechanical layout of the mechanism is demonstrated and features of the construction are shown.

4. The magnetic tape is read on a special tape reader. The conversion of the numeral code from double-decimal into a decimal system and control of tubes is brought about by electronic circuits.

5. The exposed film is developed, fixed, washed, and dried on machine 60P-1 at the rate of 180 meters/hour. From the photo-film, the calculated results are reproduced by a special automatic projector on rolls of printing paper, enlarged 3.6 times, at the rate of 600 meters/hour. The photo-paper is finished on frames.

6. Considerable increase in speed of output mechanisms can be attained with use of nonmechanical means of recording.

XVIII. Kobelev, V. V.—Engineer

Stability of Performance of Magnetic Two-Cycle Shift Registers

1. Stability of performance of shift registers is an important operation factor which, with the exception of brief mention, has not been elucidated.

2. A method of computing the process of the transmission of magnetization from one core to another in a two-cycle shift register has been found, omitting the examination of time relationships.

3. On the basis of this computation, curves have been plotted, giving the relationship between the initial and final values of current in magnetic cores, which permits demonstrating the ranges of initial currents, in which "one" and "zero" in the register are stable.

4. The relationship of the stability of the register to ampere turns of the shift pulses is examined, as well as their sharpness and relationship between the turns. It is demonstrated that a period of one time constant of one pulse brings about the stability of the register's "zero."

5. The effect of the slope of the hysteresis loop on performance of the shift register is examined in various suppositions regarding processes occurring in the magnetic material, when the condition of the material is characterized by a point lying within the limits of the hysteresis loop.

XIX. Laut, V. N.—Engineer

Circuit Methods of Increasing the Storage Time of Storage Tubes and Calculating Device with Short Damping Time

1. The physical process of storage and conditions that favor it are examined.

2. The possibility of decreasing the storage time several times (5 to 10 times) is proved with a simultaneous improvement in other parameters of the display tube by combining the optimum recording and computing method of operation.

3. Experimental data for several tubes are given for storage in the usual and improved ways.

4. The circuit of the read-write device is demonstrated, for tubes with recovery time of not more than 4 μ/sec. The circuit is not sensitive to the change of frequency, the tube, and information recorded in it.

XX. Liubovich, L. A.—Engineer

BSEM Memory Using Electron-Ray Storage Tubes

The memory mechanism (ZU) of the BESM uses special cathode-ray storage tubes with modulation on the signal plate. The ZU is parallel in operation with 39 bits and 1023 memory cells, and it consists of 1073 tubes, 231 diodes and 39 cathode-ray tubes. The maximum rate of operation is 80 kc. The deflection circuit of the tubes works on the principle of addition of equal stabilized currents, reaching the normal voltage in 2.5 μ/sec. For increasing the dependability of storage, an automatic regulator is used, first on one reading signal and then on one reading circuit, before recording. The modulation of the beam is centralized with the galvanizing unit. For the subsequent regeneration of the raster, time is used, which does not depend on the ZU cycles. The dependability of operation is checked by test programs and an automatic control. The power for the tubes is supplied from centralized stabilized current sources.

For increasing the useful operation time, spare tubes are used and preliminary checking of tubes and their chassis is carried out. The operation has shown sufficient dependability of the device (one-to-two spare tubes per day). In regard to its parameters, the given memory device is on a level with similar foreign-produced devices.

XXI. Malinovskii, B. N.—Candidate Technical Sciences

Devices Based on Combination of Magnetic and Crystal Elements

1. At present time relaxation oscillators, shaping and flip-flop circuits, based on the use of N- or S-shaped V-I characteristics of point-contact crystal triodes, are widely being used. These devices can be obtained by the application of capacitance and inductance. Devices that use capacitance have by now been sufficiently described in the literature. Systems that use inductance, having a series of specific properties, are of interest here.

2. The use of a magnetic choke permits obtaining a relaxation oscillator of variable frequency, a pulse-former of variable duration and other devices. These devices are also very convenient in experimental work.

3. Inductance can be used in the flip-flop system.

4. Experimental and theoretical studies of the oscillator with inductance in the base circuit indicate that:

a) There is a straight relationship between the oscillation frequency of the oscillator and the amount of inductance;
b) Spacing of the generated pulses does not change with change of inductance;
c) Spacing can be varied by varying voltage in the base circuit.

5. The results obtained can be applied in the analysis of the given type of mechanism.

XXII. Mamonov, E. I.—Candidate Technical Sciences

Optimal Speed of Operation and Other Technical Properties of Operating Storage Devices of Electronic Digital Computers

Given a specific length of time for arithmetic operations to be performed on the arithmetic unit (AU), one can select the optimum time relationship between the waiting period of the operating storage device and the time taken for the operation to be performed in the AU, which would assure a satisfactory calculation time. Ratio of the time taken for the arithmetic operation to the waiting time indicates what part of the total operation that takes place in the AU is waiting time and what is the efficiency of the storage devices.

In computers in operation at the present time, there are needed several storage cycles for each AU operation. There is an optimum ratio of the two times, above which value no substantial increase in the calculation time is noticed.

A comparative analysis of operation of different high-speed storage devices shows that devices employing cathode-ray tubes and magnetic cores have the shortest waiting periods (6 to 12 μsec). An appreciable increase in average capacity can be obtained by employing magnetic discs or magnetic drums. However, storage devices based on cathode-ray tubes are most widely used.

Of the various types of cathode-ray tubes, the following found practical applications in digital computers:

a) Oscillographic tube (based on Williams' system of application);
b) Barrier-grid cathode-ray tube;
c) Internal-potential-regeneration tube.

With respect to such characteristics as: storage capacity, frequency coefficient, etc., the internal-potential-regeneration tubes are inferior to the other types. In other characteristics the oscillographic cathode-ray tubes are more practical, however.

XXIII. Nechaev, G. K.—Candidate Technical Sciences, and Malinovskii, B. N.—Candidate Technical Sciences

Analysis and Study of Flip-Flop Circuits Based on Point-Contact Transistors

1. In using point-contact transistors the flip-flop element can be built using either one or two transistors. In the materials published, no detailed analysis of possible types of operation of the systems and no optimal variant are offered.

2. In examining base-controlled flip-flop systems, it would be advantageous to make use of the fact that voltage depends on current. Different types of triodes used in circuits with the same parameters will result in different characteristics. They can be classified, according to their appearance, into two categories: the S-shaped and the loop-shaped characteristics.

3. The flip-flop circuit with counter input consisting of two point-contact transistors works in a manner analogous to a tube-flip-

flop, but differs from it in that it can have three and even four stable resistance stages.

4. Comparison of different types of flip-flop that were built using two transistors shows that:

a) For practical application, operation with three stable states is recommended;
b) For the flip-flop operated in this manner, it would be advantageous to use triodes with S-shaped characteristics.

5. In the base circuit of triodes, inductance can be introduced which would permit:

a) Avoiding use of capacitance in circuits with mutual coupling;
b) Increasing sensitivity of the flip-flop.

6. A flip-flop employing transistors of the S2V (KS-8) type with loop-shaped characteristics appears to be promising.

XXIV. Ofengenden, R. G.—Engineer

Magnetic-Drum Memories

In this work, dependence of resolving capacity and amplitude of the output voltage on different parameters of the recording track was studied, and pulse erasing was investigated. By resolving capacity one means the maximum possible number of bits recorded on a single pulse carrier length.

On the basis of experimental and theoretical data, it is demonstrated that by increasing the clearance between the drum surface and the reading head the resolving capacity is decreased. Formulas are given for determination of resolving capacity and amplitudes of output pulses with noncontact writing. Experimental studies have been conducted on dependence of the resolving capcity and amplitude of the output pulses on the size of the gap and length of the writing pulses.

As a result of the examination of the pulse erasing, reasons for the small signal-to-noise ratio have been clarified and methods are given for erasing by which the signal-to-noise ratio can be increased up to 10 to 20.

Experiments were carried out on the recording of high-frequency pulses. An experimental machine was created on which recording of pulses of frequencies up to 500 kilocycles was produced.

XXV. Rameev, B. I.—Engineer

Standard Elements of Digital Computers

1. *Introduction:* General ideas on construction of electronic circuits for digital computers. Standard elements of the computer.

2. *Basic Parameters:* Determining the type of standard elements: high-speed and dependability. Adequacy of these two parameters.

3. *Essentials and Construction of Standard Elements:* Examples of construction.

XXVI. Trubnikov, N. V.—Candidate Technical Sciences

External Equipment of High-Speed Automatic Digital Computers

The external equipment of automatic computers includes assembly apparatus for preparation and input of initial data needed for the solution of a problem on the computer, and storage of results obtained by the machine.

Functions of the external equipment and its essentials. Organization and performance of external computer equipment. Speed of external equipment and its connection with the computer.

Information carriers. Aspects of carriers. Punched cards. Punched tapes. Magnetic tape and magnetic wire. Film-tape.

Composition and unification of external equipment.

XXVII. Tiapkin, M. V.—Engineer

Magnetic-Tape Memories in Contemporary Universal Electronic Computers

1. Recently there has been a tendency to use magnetic-tape memories more often (more compact recording, decrease in starting and stopping time). Consequently, one demand for an accurate tape-winding device, the read-write heads, and a stronger magnetic tape is increased, and the actual construction of the tape-winding device becomes more complicated.

2. The demand for a minimum of equipment and sufficient speed of operation leads to the parallel-series, 4 or 8 track principle of code recording. The number of auxiliary tracks must at the same time be kept at a minimum. The short acceleration time of the tape leads to the necessity of using synchronized writing pulses, read off the tape, which complicates the construction of the head.

3. The increase in the compactness of a record is due to the improvements in parameters of the tape and magnetic heads, and to the reduction in the recording level. The "nonreturn-to-zero" method, all other conditions remaining the same, results in doubling the compactness.

4. Two methods are employed for the automatic control of the accuracy of operation: the odd-number-of-pulses-in-one-line test, and summation-of-the-codes method. The first method is more complicated and preference must be given to the second one.

XXVIII. Fedorov, A. S.—Engineer

Magnetic Memory

1. The ferrite-cores memory has a short switching time. The accepted system of reading of numbers allows simultaneous reference to all bits of one number, the selection currents having no effect on other numbers stored in the memory. This system permits the reading of bits by forced operation which leads to an increase of the output signal and decrease of selection time.

2. The utilization of two cores for each bit in memory circuits considerably increases the dependability of the memory and decreases the need for magnetic-core selection in comparison with other known memory devices.

3. In the memory circuits effective methods have been devised which would eliminate interference of the writing signal with the input of the reading amplifier, thus allowing the problem of reading the signal to be solved comparatively easily.

4. The accepted system of interchanging the selection circuits allows a considerable decrease in the amplitude change of the output signal which depends on the information stored in a given bit.

5. The model of the magnetic memory is checked with simultaneous operation of the BESM. Results of the operation of this model leads to a conclusion that memories of this type have sufficiently high dependability.

XXIX. Shkabara, E. A.—Candidate Technical Sciences

Pulse Demagnetizing of Ferrites With Square Hysteresis Loop

1. The characteristics of pulse-operated ferromagnetics substantially differ from their static characteristics. Coercive force effect plays the main role in the change of characteristics of ferrite cores.

2. The present study was conducted for the case of demagnetizing with current pulses. The form of demagnetizing current pulses shows substantial influence on the processes occurring in the core.

3. When the load impedance equals infinity, it can be shown that the demagnetization time is a function of current pulses and core parameters.

Slope of the ascending section of the hysteresis loop can be estimated by the ratio of increase in inductance to the voltage increase. When one input pulse is very steep the change in slope of the hysteresis loop has practically no influence on the demagnetization time.

4. Similarly, the EMF induced in the core coil during demagnetization (if it is to be considered constant during this time) can be expressed analytically.

5. The analytically calculated values of the demagnetization time and the values of EMF, vary by 10 to 15 per cent from those taken off the experimental curves. By increasing the slope and eliminating small inaccuracies in the experimental curves one can conclude that the magnetic relaxation time increases with decreasing magnetizing field.

6. By decreasing the duration of pulses to a certain value and increasing the demagnetization frequency to 500 kilocycles, the width of the hysteresis loop stays practically constant, although its length and the slope of the ascending path decrease considerably.

7. On the basis of the experiments performed one can recommend for the design of pulse circuits in connection with ferromagnetic cores, using pulses with time constants smaller than the magnetic relaxation time, to make the length of the magnetizing pulse equal to about 3 to 5 times the magnetic relaxation time and the amplitude corresponding to about 3 to 5 times the coercive force of the given core.

B. Application of Machines

XXX. Abramov, A. A.—Candidate Phys., Math. Sciences

Solving of Large-Scale Linear Algebraic Equations on the BESM

Several problems with 200 to 300 unknowns were solved on the BESM (the problems arose in connection with geodesy). Some of these problems were over-determined and were solved in consideration of the need of the minimum sum of squares of error without transition to the normal system of equations. The problems were

peculiar in that a large number of coefficients equalled zero. The systems were solved by the iteration method. The extremely slow convergence was overcome by special procedures. The necessity for a large number of auxiliary operations (arithmetical, and especially operations using magnetic memory) greatly decreased the effective performance of the BESM.

The way in which the problems were solved leads one to believe that in design of specialized machines for solving systems of linear algebraic equations by the iteration method, it is absolutely necessary to consider the mechanization of methods for speeding up the convergence.

XXXI. Bel'Skaia, I. K., and Mukhin, I. S. —Candidate Phys., Math. Sciences

Automatic Translation From English into Russian on the BESM

1. *Construction of BESM:* The BESM has shown itself to be a powerful aid to scientific research. The solving of logical problems is a new stage in the utilization of electronic computers. The automatic translation from one language into another is an example of solving a logical problem. BESM permits investigation of the logical circuits of the translation and working out of the principles for the construction of a specialized translation machine. The experiment was a translation of a scientific article from English into Russian on the BESM.

2. *Basic Principles of Automatic Translation:* Basis for translation capability. Substitution of letters for numbers. Introduction of text.

3. *Creation of a Special Dictionary:* Words of single and multiple meaning. Grammatical peculiarities of words. Possibility of supplementing the dictionary. Specialized dictionaries for various areas of science and technology. Scope of dictionary.

Division of the translation process into two main sections: analysis and synthesis. The substitution of English words by their equivalents is the result of application of the English part of the dictionary. Dichotomous systems of analysis. The determination of grammatical forms of Russian words is the result of analysis of the English sentence and is expressed with the aid of characteristics of the equivalents. Change of the grammatical form of Russian words, taken from the dictionary, in correspondence with characteristics of equivalents is the result of application of the system of synthesis of the Russian sentence. Change to letters and delivery of translation.

Degree of change of separate parts of the translation program for texts of various areas of science and technology. Usefulness of the synthesis schemes for translation from various languages. Possibility of supplementing the dictionary with the aid of the machine.

Examples of translation from English text.

XXXII. Volkov, E. A.—Candidate Phys., Math. Sciences

On Increasing The Rate of Computation of Elementary Functions on the BESM

In solving some difficult problems on the BESM, about half of the over-all calculating time, and sometimes even more, is taken up by the computation of elementary functions according to standard subroutines. Therefore, the increase in the rate of computation of elementary functions has considerable practical interest.

The existing standard subroutines of the BESM are not optimal in relation to the time taken for computation of elementary functions.

There are three methods that can shorten the computation time of many functions. First, the range of the change of argument should be considerably decreased. Next, on the given section of the change of argument, the function should be approximated by the most suited polynomial which contains fewer members than, for example, part of a series which assures the same accuracy. And finally, the polynomial obtained should be computed directly (without cycle) by Horner's series.

Partially, by using the DZU (diode memory) 8 additional cells for the subprogram of computing logarithms, and 12 additional cells for the subprogram of computing indicating functions, the time for computing logarithms can be cut in half and the rate of computation of the indicating function can be cut by approximately 2.5 times. In increasing the length of the existing subprogram for computing the function "arctangent" by approximately two times, the rate of its computation can be increased by 12 times. In practice, it is possible to increase the rate of computing the trigonometric functions by about two times.

XXXIII. Gavrilov, M. A.—PhD Technical Sciences

Analytical and Graphical Method of Decoding Synthesis

1. Synthesis of decoders requires the solution to the following problems:

a) Selecting the most efficient and the most reliable system of signaling;
b) Selecting technical means which permit a system of signaling codes with the smallest number of elements.

2. The problem of obtaining an efficient signaling system leads to the selection of a combinatorial system in which a given number of signals can be transmitted with the least number of pulses. One should distinguish between complete and incomplete elements of combination. The means at the disposal of the designer (connection channels, pulses, and their physical properties used for combination) can be reduced to complete and incomplete elements of combination by analyzing binary tables which characterize the physically realizable combinations.

3. The problem of obtaining reliable signal transmission leads to selecting those combinations which would not result in overlapping of two signals. Signal systems may be error detecting or error correcting. The qualitative investigation of the choice of system can be aided by graphs representing selected signals in the form of loops, and the possible crossovers between them due to given errors in the form of branches. The quantitative estimate of reliability of transmission requires a stability analysis. It must be mentioned here that in both cases it is necessary to take into account not only interference in the transmission channel, but also errors produced by damaged elements of coding and decoding devices.

4. The decoding devices with error detection belong to single-cycle relay systems and those with error correction to multicycle systems. The quantitative relationship between the number of complete and incomplete elements of combination, and the number of signals, is determined on the basis of analyzing binary tables which characterize the signaling system. The effectiveness of the signaling system increases considerably if the physical properties of the pulses used for selection are combined. General questions of constructing signaling systems with error correction have not yet been investigated, with the exception of a few systems described in the literature (Hamming, Wagner).

5. The problem of constructing a relay circuit to realize the signaling system is related to the theory of relay circuits and presents, in principle, a problem of constructing the $(1, K)$ pole. There are a number of methods for solving this problem (analytical, graphical, tabular). The writer proposes a method based on pseudo connection formulas. The use of this method makes possible, in the application to flip-flop elements, a system needing only one switch for each of the elements. This gives a direct method of substituting electronic and diode devices in this application. For circuits with electromagnetic elements, the application of combinations based on coils appears to be the most promising.

XXXIV. Ershov, A. P.—Assistant of Sciences

The Program-Assembling Program for BESM of the Academy of Sciences, U.S.S.R.

The preparation for the task of program-assembling a program (PP) consists of composing a logical scheme of the program, *i.e.*, by representing the problem in the form of a sequence of several types of standard "operators." Every such operator represents the solution of some standard problem. PP distinguishes the following types of standard operators: arithmetical operator A, logical operator R, cycle, and nonstandard operator N.

The PP consists of three parts working in sequence, PP-1, PP-2 and PP-3. PP-1 successively processes operators A, R, and N, sends the formulas of arithmetical operators into the prepared program (this results in the most economical operation of working cells within the limits of one operator), prepares orders for control transfer, activating the logical operators, while the operator N is transferred without change into the program. PP-2 processes the cycles, formulates all orders relating to the cycle, forms constants, transferring address, and initial form of the transfer orders, while at the same time all the orders related to the program are received in corresponding addresses. PP-3 assigns the memory, formulates final composition of the program, and finally prints the completed program.

The PP described contains 1500 commands and is a second variant of the program, composed in October, 1955–January,

1956. The first variant was worked out in October 1954–April 1955 by L. N. Korolev (PP-1), A. P. Ershov (PP-2), and A. I. Sragovich (PP-3).

The following are the perspectives on the development of this trend in automatic programming:

1. Use of prepared standard programs.
2. Transmission to the machine for formulating the program based on a system of calculation resulting from the need of having a better type of program.

XXXV. Zhogolev, E. A.—Assistant of Sciences

Performance Test of the M-2 Computer with Automatic Scaling

This report is dedicated to some questions of programming by the "floating-scale" method, in operation with a fixed point.

The nature of the "floating-scale" method, applied to a series of problems by collaborators of the Computing Center of the Moscow State University (MGU) on the machine M-2 ENIN AS USSR, lies in the fact that some of the figures are stored in two cells of the memory: in one the "mantissa" and in the other the "characteristic" (or "scale") of the number; during computation the necessity arises of changing the scales of some of the values, which is done automatically by the program.

Standard subprograms of basic elementary functions composed at the MGU for the given method are examined: subprograms for transforming from the decimal system of computation into the binary and vice versa.

In addition, programs for integration of differential equations by the Runge-Kutta method with the Gill modification are examined, when the right-hand sections are polynomials of unknown functions, and also when the right-hand sections represent fractions of trigonometric polynomials.

Comparison of programs with floating point is carried out, and advantages and disadvantages of both methods are demonstrated.

As an example of the solution of algebraic equation by Lobachevsky's method, advantage of the "floating-scale" method over one floating-point method is shown.

XXXVI. Karmazina, L. N.—Candidate Phys., Math. Sciences

Computation of Tables on Computers

1. Since 1952 a series of "Mathematical Tables of ITM and VT AS (Academy of Sciences) USSR" has been published.

The type of work on the tables is such as to require a large number of derivations and handling of numbers.

Computation, control of tables, their preparation for publication, and the correction process is done on computers.

In the system of direct solving of all tabular functions, the computations of the tables on the BESM is not very efficient. The possibilities of SAM for the computation of tables are very limited.

2. The tables are computed and their preparation for publication and correction is done with the help of punched-cards. Their preparation and control is done on the SAM; the basic method of control is in the checking of differences.

3. Up to now the tables have been published by means of typographical typesetting and, therefore, there is much labor involved in correcting. The corrections are conducted manually on controllers. The photo-offset methods of publication of tables are considerably more dependable and economical, but this is difficult in the absence of essential equipment.

4. Problems:

a) Development of methods of computation of tables, permitting a more effective use of existing computing techniques and construction of specialized machines.
b) Application of computers for computation of tables.
c) Automation of labor connected with publication.

XXXVII. Katskova, O. N.—Assistant of Sciences, Chushkin, P. I.—Assistant of Sciences, and Shmyglevskii, IU. D.—Assistant of Sciences

Some Problems of Gas Dynamics

1. Calculation of streamlines around static and rotating bodies of gas flowing at a velocity approaching that of sound (P. I. Chushkin).

For the solution of this problem the method of integral relationships is applied, which has earlier been proposed by A. A. Dorodnitzyn. The equations of continuity and laminarity, plotted in elliptical coordinates, are integrated along the coordinate which changes along the hyperbolas from limits of the streamlined body to infinity. In the integral relationships obtained in this manner the subintegral functions are approximated by polynomials along this coordinate. Then the problem is simplified to the marginal problem of the system of ordinary differential equations along another coordinate.

By means of repeated integration of this system on an electronic computer, a solution is obtained, satisfying boundary conditions. This can be done automatically by a special program. The nature of the relationship of integrals to lines, which lie between the limits of the body and infinity, permits raising the accuracy of approximation and making a more precise approximate solution.

Critical Mach numbers for ellipses and ellipsoids of revolution were determined by a similar method. As an example, Zhukov's streamlines for near-sonic gas velocities and streamlines for gas at sonic velocities flowing around elliptical bodies were calculated by this method.

2. The axially-symmetrical supersonic current of freely expanding gas with a flat crossover surface (O. N. Katskova and IU. D. Shmyglevskii).

The usual equations of gas dynamics are converted to new coordinates—to the current functions and the characteristic change, changing along the first family characteristics.

In the region of crossover surface the solution of unknown functions (Mach's angle, the angle of rate incline and distance from a point to the axis of current) is in the form of gradual series determined by the characteristic variable. For obtaining a solution in the remaining supersonic region of gas flow the method of characteristics is applied. In the neighborhood of the axis of the stream the symmetrical-axis relationship of the characteristics is found to be undetermined.

Getting a sufficiently accurate solution is connected with very cumbersome problems which were solved on the BESM. Solution of the problem examined depends on the ratio of constant pressure and constant volume values of specific heat. Tables of the unknown functions were calculated for the following values of this ratio: 1.14, 1.33, 1.40, and 1.666.

XXXVIII. Koroliuk, V. S.—Candidate Phys., Math. Sciences, and Iuschenko, E. L.—Candidate Phys., Math. Sciences

Determination of Level of a Function of Two Variables on High-Speed Electronic Computers

In order to determine the level of a function of two variables a method of tracing at a fixed rate along the sides of the parallel lines mesh is employed.

The accepted method of tracing comprises a simple and economical process on a high-speed electronic computer, which determines the height of the squares, having common points with the level line.

XXXIX. Kulagina, O. S.—Assistant of Sciences

Translation from French into Russian on a Computer

1. Working out of the algorithm of translation.

2. Composition of a dictionary for computer translation:

a) Selection of translations;
b) Character of dictionary information;
c) Dictionary of phrases.

3. Structure of translation algorithm:

a) Principle of dictionary search;
b) Working out of phrases;
c) Differentiation of homonyms;
d) Group of analyzing rules;
e) Character of information on the phrase translated and obtained by analyzing rules;
f) Group of synthesizing rules.

4. Grammatical features of computer translation:

a) Division of verbs into groups;
b) Sentence codes.

5. Structure of translation program:

a) Operational order of translation rules.

XL. Liubimskii, E. Z.—Assistant of Sciences, and Kamynin, S. S.—Laboratory Assistant

Automation of Programming

1. *Program-Assembling Programs:* The program-assembling program is an example of preparing a difficult problem for solution.

The given problem is defined as an algorithm task, and different algorithms for manual and automatic computation are examined. The necessity of expanding the algorithm is underlined and its nature studied.

Generalized orders (operators) are introduced as well as the outline of the program based on the expanded algorithm. The automation methods of translating the generalized orders into the "computer language" are studied. A number of algorithms of the program-assembling program are proposed and its operation analyzed.

2. *Further Ways of Programming Automation:* Various automation methods of programming with the aid of standard subroutines and subprograms and the automation of expanding the algorithms are studied.

Investigated are the programming principles of the composed system and of the memory-allotting program.

3. *Automation of Control:* The need for control in different stages of the programming automation is investigated, together with ways of controlling and making the control automatic.

XLI. Liapunov, A. A.—PhD. Phys., Math Sciences, and Ianov, IU. I.—Assistant of Sciences

Logical Schemes of Programs

1. Necessity for dividing the programming process into more automatic stages.
2. Separation of elementary operators and basic control parameters. Construction of the program system.
3. Control operators and their basic types. Transition from the system of computing to the program system.
4. Method of constructing a program with a given system.
5. Change of the computing and program system as a means of improving the final program.
6. Concept of the algorithmic systems.
7. Identical conversion of algorithms for improving programs.
8. On the use of the program systems in some problems of cybernetics.

XLII. Purto, V. A.—Candidate Philological Sciences, and Moloshnaia, T. N.—Assistant of Sciences

Computer Translation from English into Russian (Some Linguistic Problems)

1. History of the problem of computer translation abroad, and its solution.
2. Computer translation from English into Russian and problems related to it.
   a) Necessity for a formal analysis of the grammatical structure of the language in computer translation.
   b) Comparatively small number of word measuring affixed in the English language. Lexico-grammatical homonymy.
   c) Selection of the homonymy as a necessary condition for the correct analysis of the English, and construction of the Russian phrase.
   d) Methods of analyzing the English sentence:
      (1d) Classification of English words according to form.
      (2d) Distinction of typical structures of English sentence.
      (3d) Analyzing the sentence by first subdividing it into distinct two- or three-word units and then analyzing them subsequently.
      (4d) "Transforming" the analyzed English sentence into a Russian sentence.
   e) Possibility of additional checking of the translation by applying Bar-Hillel's method.
      1) Classification of English words into nouns and predicate words. Index principles.
      2) Service words and their indexing.
      3) Representation of the structure of the English sentence by the accepted index.
      4) Checking the selected indexes by analyzing the final translation after simplification; possibility of applying homonymy.
   f) Methods of compiling a dictionary for computer translation from English into Russian, taking the peculiarities of English language as well as the rules for analyzing an English sentence into account.

XLIII. Rameev, B. I.—Engineer

One Method of Evaluating the Reliability of Electronic Systems of Discrete Action

1. Reliability is one of the basic factors of computer. Several papers are known which investigate the questions of reliability of various systems. A common method of estimating is essential.

2. The subdivision of electrical circuits, depending on the mathematical method used for their analysis, into linear and nonlinear circuits, does not fully characterize the circuits. Knowledge of the type of change of the variables can result in change of the method of analysis of a given electric circuit.

It is advantageous to divide electric circuits according to the type of change of their variables into systems of discrete and continuous action.

The relationship between input and output of a system of discrete action is controlled by the logical function and, in contrast with systems of continuous operation, it can be depicted by the system exactly. Accuracy of a discrete-action-system is quite distinct: the system either functions correctly (and the performance of the operation is absolutely exact), or does not function correctly (the performance is completely wrong).

A system can be called reliable if any permissible change in element parameters, including change in supply voltages, does not affect solution of the logical equation.

Consequently, the study of practical discrete-action circuits may serve as the subject for determining reliability of continuous-action circuits.

a) To determine reliability for a given circuit, with certain deviations of parameters (tolerances) of all input signals into the circuit and variations in power-supply voltages (direct problem or circuit analysis problem).
b) To determine permissible variations in parameters for a given circuit and variations in their supply voltages, with given reliability of the circuit (indirect problem or circuit synthesis problem).

3. When the main dependent function is interrupted, relatively large values of deviation in the parameters (10 to 30 per cent from the nominal) occur, the propositions and methods of calculation of known theories of accuracy are not applicable in the investigation of electric circuits of discrete action.

The calculation of reliability of one very complex system of discrete action can be simplified to the calculation of reliability of a number of much simpler systems.

Some additions to the known methods of calculation with the aid of volt-ampere characteristics make the graphical method of determining voltages at different points sufficiently complete and general for the calculation of very complex nonlinear electric circuits.

The simple rules permit the analysis of nonlinear circuits, taking into account the deviations in parameters. The calculation can be done for very poor as well as for reasonable element tolerances.

4. It is advisable to use nomograms in order to simplify and speed up the calculations. Solutions for both direct and indirect types of problems is possible.

5. The basic rules for constructing the volt-ampere characteristics for simple and complicated circuits with variation in parameters. Evaluation of errors in this method of analysis.

6. Examples of analyses of various circuits.

XLIV. Shreider, IU. A.—Candidate Phys., Math. Sciences

Monte-Carlo Method

The algorithmic system given by the Monte-Carlo method for the solution of a series of very important problems, makes it necessary to store a small number of intermediate results.

The error obtained in the solution by the Monte-Carlo method is determined by the number of trials. Errors due to rounding off figures and arithmetical errors in separate trials do not substantially influence accuracy of the solution. It is possible to obtain accuracy to about three decimal figures.

The Monte-Carlo method is applied to problems which do not demand great accuracy, but the problem itself may be of a complex structure. This refers primarily to boundary-value problems for partial differential equations, multiple integration, and the solution of integral equations. Particularly convenient are problems of probability type: problems connected with distribution theory, passing of particles through a substance, and ballistic problems. A series of problems, the solution of which by usual methods calls for great calculating difficulties or which is in general unrealistic at present, can be effectively solved with the aid of the Monte-Carlo method.

For the realization of a method, the existing computers can be used, and their effectiveness can be increased by construction of special attachments. But it is more effective to construct specialized computers solving either a separate class of problems by the Monte-Carlo method, or permitting the solution of a broad class of problems by this method (universal-type computers). The last two types of computers must be substantially simpler than general-purpose computers.

XLV. Shura-Bura, M. R.—PhD. Phys., Math. Sciences, and Trifonov, N. P.—Candidate Phys., Math. Sciences

Programming Test and Solution of Several Mathematical Problems on the M-2 ENIN AS USSR Computer at the MGU

The Moscow State University (MGU) has been regularly operating the M-2 computer simultaneously with the ENIN AS Academy of Sciences USSR since the end of December 1955.

The topics of the proposed problems are very broad (systems of simultaneous differential equations, the search for extremes of a function of three variables, systems of linear algebraic and transcendental equations, calculation of improper integrals, composition of tables, etc.); however, in all the problems there are many parts resembling each other. Therefore, it was decided to construct a library of standard subprograms.

It is agreed that in the majority of cases operation with a fixed point and constant scales is not realistic, and, therefore, the machine is operated either with a floating point or with a fixed point with "floating scales."

Consequently, the library of standard subprograms is composed of two parts, applicable to each of these types of operation. (There will be a separate report on operation with floating scales.)

An input program is prepared which controls the correctness of input information from punched-tape and assigns to the standard subprograms and to other material corresponding locations in the memory.

The method for preparation of problems is still poorly worked out. Solution of problems according to prepared programs is conducted, as a rule, by engineers without the aid of mathematicians.

XLVI. Eterman, I. I.—Candidate Phys., Math. Sciences

Programming Features of the "Ural" Computer

Purpose and brief description of performance of the "Ural" computer. Form of presentation of numbers, size of the display, storage capacity, temporary parameters, external apparatus of the machine.

Operational composition and structure of orders. Some operational features of the machine. Examples of simple programs. Approximation formulas and programs for the realization in the machine of some elementary functions. Special features of programs for machines with fixed-point operation. Examples of working programs for the solution of problems on the "Ural" and their parameters (storage capacity, number of orders, solving time, etc.).

Special programming methods for utilization of subprograms for floating-point operations, automatic correction of scales, and scale coefficients.

Characteristics of test programs and methods for controlling accuracy of performance of the machine.

XLVII. Iablonskii, S. V.—Candidate Phys., Math. Sciences

Multi-Valued Logic and Electric Circuit Theory

In application one often comes across devices which have, in general, n inputs and m outputs, each of which can appear in one of k conditions; at the same time the conditions of the output channels are determined by the conditions of the input channels. The condition of these channels can be characterized by whole numbers such as 0, 1, 2, $\ldots$, $k-1$. Evidently the operation of these devices is described by the accumulation of some m functions of n variables in such a way that the values of the arguments indicate the state of the input, while the value of the function indicates the state of the output. The aggregate of all such functions forms the k-valued logical expression.

Functions may be presented with the aid of tables. However, such a task is connected with cumbersome recording even in the case of $k=2$ (*i.e.*, logical algebra) and a rather small n. The problem arises of representing the function of the k-valued logical expression with the aid of formulas composed of any number of simpler elementary functions.

It is known that any function of the k-valued logic can be written down in a formula composed of functions of such systems. Such formulas can be interesting also from the point of view that in some cases they give a picture of the circuit.

In connection with this arises the problem of separating all these systems from the k-valued expression, which would represent any function of this expression in the form of a formula (problem of completeness). The completeness problem has been completely solved. It becomes evident that from any such system (complete system) one can select a complete subsystem consisting of a finite number of functions. However, even in this case, the over-all solution is impractical.

In the case of arbitrary k, one can show a number of effective criteria of sufficient completeness. They are all based on the concept of the so-called closed type.

The effective criteria for $k=2$ were obtained by one method and for $k=3$ by another. In these cases, the completeness problem allows for a complete solution. It also becomes evident that for $k=2$ one can select from any complete system another complete system with not more than four functions, and for $k=3$ with not more than seven functions.

C. Specialized Machines Chairman—Corresponding Member V. A. Trapeznikou

XLVIII. Bedniakov, A. A.—Engineer

Electro-Mechanical Differential Analyzer

General characteristics of the machine and its structural features.

Characteristics of the basic mathematical units of the differential analyzer (integrating, function forming, adding, multiplying), their constructional features and accuracy in forming a function and performing an operation.

Automatic adjustment, control and regulation: commutation of devices, introduction of problem conditions, control of accuracy of adjustment, introduction of an independent variable, and system of automatic speed regulation, controlling systems, delivery of result.

Basic steps in problem preparation for solution on the machine: transformation of equations into a form suitable for solution on the machine, calculation of parameters of the system, calculation of scale and scale coefficients.

Testing solution of several problems on the machine and comparing instrumental solution with numerical one.

Basic methods of controlling the accuracy of performance of separate mathematical units and the machine as a whole.

XLIX. Belikov, IU. N.—Engineer, and Rameev, B. I.—Engineer

Specialized Automatic Computer of the "Crystal" Type

1. *Introduction:* Problems solved on the "Crystal" computer: calculation of electronic compactness, structural amplitudes, and the value of the p^2 parameter. Basic formulas, possible types of solution, range of variations in initial data.

2. *Basic Parameters of the Machine Pertaining to Operational Techniques:* General characteristics of the machine. Time of solution of 1, 2, and 3 problems with different range of variations in the initial data of the problems.

3. *Composition of Machine and Features of Separate Devices:* Block diagram of machine. Devices for input of initial data and delivery of results, and their features (automatic conversion, control, speed of operation, etc.)

Functional construction and its features. Computing values of trigonometric functions. Reduction of angles to the first quadrant. Working out the value of the function $\psi(p^2)$. Calculation of atomic weight. Computing the values of index h, k, and their product.

4. *Performance:* Process of solving of problems on the "Crystal" machine.

L. Vin'kov, M. P.—Assistant of Sciences, and Kalashnikov, V. A.—Assistant of Sciences

Performance Test of EV-80-3 Electronic Computer

The performance test of the electronic computers in Central Aero-Hydromatic Institute (CAGI) and in Moscow State University (MGU) demonstrated that these machines have a series of serious performance inadequacies due to poorly designed technological plans and poor construction of different units and details.

The basic defects of EV-80-3 are:

1. Inadequate memory capacity;
2. Impossibility of obtaining full control of calculation in one run of punched cards;
3. Low reliability.

As a result of these defects, the factual productivity of the machine is merely a small percentage of the required one under these technological conditions, and the solution of problems on it, in case of shortage of time, is not possible in practice.

The production of electronic computers can be advantageous only on condition that the machine be improved in the following areas:

1. Increased storage capacity;
2. The system of the calculation control must be worked out more thoroughly;
3. The following units and blocks now working unsatisfactorily must be reconstructed: solenoids of the punching mechanism, power supply block, cascaded networks, etc.

LI. Vin'kov, M. P.—Science Collaborator

Investigation of Operational Features of Tabulators Applicable to Problems Solved in Computer Stations in Machine Construction Plants

The performance test of calculating-analyzing machines employed in the plant computer stations indicates that the performance of the tabulators does not satisfy the requirements placed on them.

1. The basic inadequacies of calculating and printing mechanisms of tabulators T-4MI and T-5 are:

a) Inadequate capacity;
b) Rigidity or inadequate flexibility of the system separating calculating mechanisms into calculators;
c) Rigidity of systems dividing printing mechanisms into sections;
d) Inability to print letters, resulting in application of numerical codes to designate symbols.

2. The inadequacies of the relay-contact system of the T-4MI tabulator are:

a) Absence of facilities to introduce numbers in the usual form or in the form of additions from one digit position of the calculating mechanism into another;
b) Absence of facilities to print numbers which are in one digit position of the calculating mechanism in any desirable position of the typing mechanism.

The main inadequacy of the relay-contact systems of T-4MI and T-5 tabulators is the inability to multiply by the tabular method, thus hindering the effective application of calculating-analyzing machines for the mechanization of norm calculations.

3. In order to eliminate difficulties encountered in solving complicated problems and in increasing effectiveness of application of the calculating-analyzing machines at the computer stations of machine-building plants, the performance features of the tabulators should be improved in the following manner:

a) Capacity of the calculating and printing mechanism must consist of 140–150 and 110 digit positions, respectively;
b) The system of dividing the calculating and printing mechanisms into calculators and sections must assure the most effective use;
c) About half of the capacity of the calculating mechanism must be adapted to converting the figures introduced into additions;
d) The left side of the printing mechanism must be capable of printing letter symbols;
e) Construction of the relay-contact system must assure performance of all functions required by the T-5 tabulator as well as multiplication by the tabular method;
f) The relay-contact system must be constructed in such a way as to assure maximum care in balancing the machine;
g) The basic mechanisms and the relay-contact system must be such, as to make the machine adaptable to automatic operation.

LII. Vittenberg, I. M.—Candidate Technical Sciences

Expansion of Possibilities of Electric Analog Computers Developed in KB MMiP

1. Device for observing and storing solutions obtained on electronic analog computers, developed in the KB MMiP.
2. Solution of boundary-value problems on electronic analog computers by the method of minimizing with the aid of an electron-ray minimizer.
3. Methods for solving systems of algebraic and transcendental equations with the aid of electronic analog computers.
4. Small electronic analog computers of the ML-2 type for solution of systems of algebraic equation with 12 unknowns.
5. Solution of integral equations of the Fredholm and Walter type on electronic analog computers by the method of successive approximations. Description of mechanism for multiple reproduction of solution.

LIII. Volynskii, B. A.—Candidate Technical Sciences

Simulation Devices For Solving Boundary-Value Problems

In recent years there has been a considerable development in connection with simulation devices used for solving boundary-value problems.

During 1950–1955, specialized electric network analyzers were developed for the solution of the petroleum problem in connection with the rational development of petroleum layers. EM-5, EM-7, and EM-8 circuits have a peculiar design of scaling system and electronic device for solving nonstationary problems. These circuits have from 2000 to 7000 junction points and permit "switching" of hundreds of wells.

The electronic analog computer EM-6 in Giproproject has been operated for more than 4 years and is used for solution of important problems in connection with determining the strength of foundations, blocks, etc.

In 1949 the first larger network analyzer was constructed with 15,000 junction points and was used to solve a magnetic problem in semispace. The network analyzer consisted of a central unit and a periphery on which infinity was simulated. Considerable error inherent in this method has led to a simulation method using integral form.

In 1955 the Institute of Exact Mechanics and Computation Technology of AS U.S.S.R. delivered the apparatus *IZ* (letters are abreviation for "Integrating Stars"), delivered for normal operation. The principle of this apparatus is based on application of integration with the aid of the integrating stars. First and second derivatives can be obtained on this machine with 3 to 5 per cent accuracy. The question of error has been examined for this method.

A series of important questions can be practically solved by the application of an array of networks, stars, and high-speed computers. This possibility needs additional examination.

Further problems in the area of development of theory and practice of the simulation devices for the solution of boundary value problems are: development of method of solution of problems by networks and integrating stars with increased accuracy; solution of three-dimensional problems; simulating of the circulation elements, latent heat, nonlinearity; examination of possibility of application of printing systems; automation of input and output devices.

LIV. Gluzberg, E. A.

Checking Procedures for Preparing and Solving Common Differential Equation Problems on Electrical Analog Computers

1. Elements of the mathematical checking apparatus for analyzing errors of electrical devices used for solving common differential equations. Examples.
2. Practical methods of analyzing influence of amplifier drifting and accuracy of introducing coefficients and nonlinear functions on accuracy of results obtained from electrical devices.
3. Comparing the results obtained with the aid of an electrical analog computer with calculated results as one method of checking reliability of electrical devices. Significance of accumulating experimental data on simulation accuracy of some types of problems. Examples.
4. Methods of checking scale computation and coefficients of transmission of blocks, as well as balancing of the functional blocks and their commutation.
5. Some experimental results of electrical analog computers in KB MMiP.

LV. Kogan, B. IA.—Candidate Technical Sciences

Application of Electronic Simulation Devices for Testing of Automatic Regulator Systems

1. The methods of simulating automatic regulation systems and their brief description. Analog and digital devices. Simulator as a computer and its place in the general complex of methods of computing technology. Tendencies and perspectives for development of these devices.
2. Requirements concerning technical characteristics and composition of contemporary electronic analog computers designed for testing automatic regulating systems. The possibility of utilizing electronic analog computers as principal parts in an automatic regulating system.
3. Principles of construction of electronic analog computers not requiring stabilized power sources. Methods of increasing the duration of solution of problems on electronic analog computers. Simulators in EMU-6, IAT, AS U.S.S.R.
4. Application of electronic simulators for the analysis and synthesis of systems of automatic regulation.

Determining stability limits. Computing the value of the mean-square error, determining connection between integral evalua-

tions and quality of the transition process, obtaining of general relationships for nonlinear systems.

Examples of testing a common nonlinear system.

Experiments with the equipment.

LVI. Kuz'Minok, G. K.—Engineer

Performance Test of Simulation Computing Equipment

1. Survey of simulation equipment (universal and specialized), developed by the Institute of Exact Mechanics and Computing Technology of the Academy of Sciences, U.S.S.R.

2. Performance Test: a) of the electrical integrator, EI-12 for the solution of Laplace and Poisson equations; b) of the simulation device, intended for the solution of equations of the parabolic type; c) of electron-tube integrators ELI-12 and ELI-6.

3. Possibilities of further development of simulating devices.

LVII. Maslov, N.G.—Engineer, and Rameev, B. I.—Engineer

Automatic Computer for the Computation of Sum of Even Products ("Pogoda")

Purpose and Area of Application: Solution of problems consisting of summation of products. Typical problem: multiplication of matrices. Problems: distribution into series and summation of series (Fourier, specific functions, etc.), solution of systems of linear algebraic equations by the iteration method (simple iteration, Seidel's method), calculation of the polynomial value by Horner's method.

Enlarged Block-Diagram of Machine

Analysis of Different Characteristics of Solution Methods: Orderly distribution of numerical data, more initial data with a relatively lower number of operations. Structure of the machine. Basic elements of the machine and their purpose. General operating diagram of the machine. Control- and number-conversion devices, and their purpose. Computation system. Conversion of numbers from one system into another together with the arithmetical operation in a special block. Operations with numbers. Block-diagram. Operation with lower-class numbers. System of orders.

Constructional Properties of the Machine: Basic parameters of the machine and their comparison with others.

LVIII. Mairov, F. B.—Ph.D. Technical Sciences

Application of Digital Integrators to Automatic Machine Control

1. The proposed layout of a digital integrator, with a synchronization-pulse frequency of one megacycle or higher, results in a sufficiently fast solution of a problem for automatic machine control.

2. Application of digital integrators assures a continuous machine control process, as well as simple and flexible balancing of the machine in solving different problems.

3. The proposed multichannel transforming and functional units make relatively easy the introduction into the integrator of different information, including voluminous tabular data.

4. The digital integrators, being compact and economical, are very well suited for various practical applications.

LIX. Nikolaev, N. S.—Engineer

Specialized Electrical Analog Circuit of the EI-S Type

Solution of underground flow problems, in connection with rational development and economical exploitation of oil fields, can be simplified to a problem of solving partial differential equations.

Static problems (water-pressure type) are reduced to equations of the Laplace type and dynamic (electricity type) problems to equations of the Fourier type. Analytic methods of solution of these equations are either for special cases (problems of Dirichlet-Neumann area of rectangle or circle), or are so complex that their practical application is difficult.

Calculation methods, in particular those of the finite-difference type, permit obtaining a solution for a wide class of equations with particular derivatives, not limiting the original data.

However, the finite-difference method requires a solution of several thousand algebraic equations. Even the application of high-speed digital computers in this case is not realistic because of the requirement of a very high memory capacity and the difficulties in the variations of parameters.

The initial data in solving petroleum problems are obtained as a result of geological research and their probable error is about 15 to 20 per cent, and consequently, the solution cannot be very accurate.

The specialized electric analog computer of the EI-S type, developed and planned in 1954–55 permits solving the described problems with a small margin of error.

The examined area is simulated by a network of active resistances, having some 13,000 points.

The expansion capacity of the layer is simulated with the aid of capacitors, connected to the junction points of the network.

The analog permits investigating a field with a positive number of 500 active and up to 250 drilled wells.

The wells are simulated by special channels, the total number of which is 750.

The channels can be automatically connected or disconnected several times during the time of solution, depending on the program.

The automatic switching of the channels from one type of limit (yield of the well) to another type of limit (pressure) can be performed in the course of solving the problem.

The variable can be simulated along a given curve during the "yield" time or the "pressure" time.

The initial conditions (voltages on the junction points of the network at the correct time) are applied to the above-mentioned capacitors by reversing their plates and connecting them to a special initial-conditions divider.

Nonstationary problems are solved on the analog computer with a frequency of 4 to 8 cps.

A time of 0.1 second is reserved to set the network to the initial conditions during the cycle of the analog computer, and during this time the circuit is de-energized with the aid of electronic switches.

The instantaneous values of these functions can be measured with compensated meters.

LX. Nikolaev, N. S.—Engineer

Application of Computers in Railway Transportation

1. To compile data for graphs in connection with railroad traffic, planning of railroad lines, new types of transportation systems, etc., it is necessary to do traction and heat calculations, as well as calculations connected with required electrical energy and wasted mechanical work.

2. The initial data of this equation are substituted into the nonlinear functions of traction and brake force which depends on speed of the train and profile of the track. By solving this problem, one should obtain graphs showing how speed and time depend on the track.

3. In heat calculations the nonlinear differential equation is solved which describes the heating up of electrical windings in electrical and thermal locomotives. The initial data of that equation are substituted into the nonlinear relationship of heat parameters as a function of electric current. Solution of this problem should result in a plot of heating of the machine as a function of the track. In order to calculate electrical energy use, a first-order differential equation has to be solved. Initial data in this equation consist of horsepower as a function of speed. This gives the amount of energy or work spent by the locomotive at certain conditions of motion.

4. Up to the present time, the heat and traction calculations were performed through graphical integration. The laboriousness of this method resulted in application of a great number of specialists and necessitated a number of simplifications which lowered the over-all accuracy.

In 1954 the specialized nonlinear electric analog computer of the ATR-1 type was developed, which was used for traction calculations, and in 1955–1956 another nonlinear analog computer ATR-2 was devised and used for heat and electrical and mechanical energy calculations. At the present time these machines are being produced in large quantities. Experiments show that these devices are sufficiently accurate for solution of the above-mentioned problems.

With application of this machine, there are enough calculating methods so that the optimum one may always be chosen.

The possibility of solving the equation of train's motion instantaneously may actually result in this method being applied to automatic control of the locomotive.

Automatic control of locomotives eliminates the influence of subjective factors, assures a more accurate plot of the train's motion, results in a more economical operation, and increases the safety of travel.

The present mechanical car-sorting tracks, present in many railroad stations, unfortunately do not permit elimination of manual labor, reduction of the spacing between the cars, and collision of cars traveling at too high a speed.

The reason for this is the absence of any automatic control of the car brakes on the

above-mentioned car-sorting tracks. Automation of this very important operation should assure safe decoupling intervals at maximum permissible velocities, and the collision of cars at the correct place and speed.

The computer calculates resistance of the car rolling on the inclined track and its velocity after it is released from the braking position, according to the profile of the track and length of the path the car has to travel before it is coupled.

The computed speed determines the braking time and braking force which is automatically transmitted to the brake.

After that, the actual measured speed after decoupling is compared with the theoretical one and the necessary correction is made by automatic braking.

LXI. Petrov, G. M.—Engineer

Small Nonlinear MN-7 and MN-10 Electrical Analog Computers

1. Brief technical description of the small nonlinear electronic MN-7 simulator:

a) Area of application;
b) Composition of basic solving equipment;
c) Specific features, distinguishing this equipment from those put out in the U.S.S.R. and abroad.

2. Characteristics of the MN-10 equipment.

LXII. Smirnov, A. D.—Candidate Technical Sciences

Performance Test of Simulators

1. Performance test of electronic simulators of the IPT-4, IPT-5, MN-3 and MN-2 types.
2. Brief description of problems which were solved on these simulators.
3. Performance inadequacies of these devices and measures for their elimination.
4. Conversion devices for electrical analog computers and objectives they have to meet.
5. Methods of evaluation of accuracy of the solution and demands for accuracy of separate solving elements.

LXIII. Sulim, M. K.—Engineer

Digital Differential Analyzer

Construction principles of digital differential analyzers: method of integration, diagram of digital integrator, diagram for increasing the integrated function as well as the function itself, diagram for increasing the independent variable.

Functional diagram of digital differential analyzer. Introduction of initial data. Introduction of tabular and experimental functions. Output devices of machine: printer, plotter.

Special types of operation of integrators: operation of adder, multiplication by a constant.

Preparation of initial data for solution of problem on digital differential analyzer; diagram of integrator coupling for solution of problem, coded tables; scale and scale correlations.

Composition and parameters of the constructed machine. Quality of the solution.

LXIV. Feldbaum, A. A.—Ph.D. Technical Sciences

Possibilities of Applying Computers For Automation of Production Processes in Metallurgy

1. *Methods of Applying Computers in Automatic Systems (AS)*: Computers used in AS can be divided into three groups: order-type computers, data-processing computers, and computers built into the closed circuits of AS. The latter type of computer is the most practical.

2. *Brief Description of Possibilities of Applying Computers in Metallurgy:* Possible areas of automation are: rolling mills, blast furnaces, open hearths, electric smelting furnaces, etc. At the present time the use of computers is primarily advantageous in such areas as the electric arc smelting furnaces and continuous sheet cold-rolling mills.

3. *Basic Trends in the Development of Computers for Automation of the Above-Mentioned Areas:* The basic trends in the development of computers are: theoretical studies of ideal systems, construction of electronic analogs of systems, application in the development of automation block-diagrams, development of the computer blocks, test of the computer equipment on an electronic analog computer, etc.

4. *Automation of Electric-Arc Smelting Furnace:* According to the data obtained from the CLA NIICHERMET and together with this organization, the basic principles of application of computers for the automation of a process are developed.

The first part includes automation of only the electric part of the furnace, in view of the absence of heat-measuring devices at the present time. The sample model of a regulator utilizing a computer has passed the test.

5. *Automation of the Continuous Cold-Rolling Mill:* The work was started simultaneously with CKB MM (Mintiazhmash) and CLA (Minchermet). One can construct an approximate equation of the process which would simplify the design of the block diagram of the automation as well as of the electric analog computer.

6. *Possibilities of Applying Computers in Metallurgy in the Near Future:* The basic difficulties are inadequate studies of the areas, lack of measuring devices, inadequacy of modern theory and existing principles of automation, inadequate reliability of computers during long operations at shop conditions. In order to overcome the above-mentioned technical difficulties, a close co-operation between government and scientific institutions is required.

LXV. Tzukernik, L. V.—Candidate Technical Sciences

Analysis of Stability of Dynamic Systems in Electronic Computers Based on The Example of Power Systems

1. According to Liapunov, the problem can be broken up into two seemingly independent parts:

a) Determination of the coefficients of the characteristic equation of the complicated regulating system;
b) Determination of the stability criteria and the stability limits of the given parameter function.

2. In order to transform the initial differential equations and calculate the coefficients of the characteristic equation, an algorithm can be devised which would program the typical logical operations and other calculations for an electronic computer. The main characteristic of such a type of programming is the use of matrices, the elements of which can represent not only numbers, but also algebraic expressions.

3. The following method is recommended for stability limits calculations:

a) The coefficients of the characteristic equation serve as initial data and are represented in the form of a function of two parameters (for instance, the coefficients of regulation).
b) During the calculation time these parameters are assigned a series of different values in sufficiently short intervals. For every pair of values the Routh's criterion is constantly calculated. While the machine is calculating, the values of the varying parameters for the beginning and end of each period during which the sign of the criterion is changed, are shown on the machine. These values determine the location of the desired point on the stability limit curve.

4. The power systems of the IE and IM AS (Academy of Sciences) of U.S.S.R. represented by three equivalent circuits whose characteristic equations were of the tenth order were analyzed on the BVM to their static stability. Automatic regulation of excitation of one or two generators on a distant station was investigated, as well as regulation of the intermediate synchronizing capacitor. It was proposed to regulate first the voltage and current variations and then additionally regulate the first and second derivatives of the current, or slip and acceleration. A number of stability regions for the regulation coefficients was obtained for the above-mentioned types of regulation. The starting conditions were also varied ($R_0=0$, 0.5, 1.0, 1.1) as well as the power system circuit (with and without distance compensation of the transmission line).

The results of base calculations agree with the results obtained from electrical analog computers in cases where there are experimental data for such a comparison.

All of the calculations were based on equations derived by the author for disturbances in complicated power systems. The programming was done by the Mathematical Institute AS of Ukranian S.S.R.

LXVI. Tsypkin, IA. Z.—Ph.D. Technical Sciences

Some Dynamics Questions of Regulation Systems Employing Digital Computers

Basic types and characteristics of regulating and control systems utilizing digital computers are examined.

It is demonstrated that a system employing digital computers is equivalent to a pulse or interrupted regulation system.

In order to analyze such dynamic systems employing digital computers the pulse-regulation theory is applied.

It is shown that by introducing digital computers into the regulation system the stability of the system is increased and optimal processes may be obtained, *i.e.*, processes with maximum and minimum regulation time in systems with and without lag.

The method of determining the program for a digital computer is explained which takes the given requirements into account.

Requirements of digital computers from the point of view of their application in regulating systems are briefly examined.

LXVII. Korol'kov, N. V.—Candidate Technical Sciences

Application of Ferrite Cores in Computers

1. High-speed digital computers designed to perform primarily logical operations, computers designed to regulate manufacturing processes, and other specialized digital computers usually consist of a very high number of elements which should be very reliable.

The basic elements utilizing ferrite cores have many advantages over elements utilizing vacuum tubes.

The basic advantages are: reliability, durability, compactness, small power requirements, and cheapness.

2. The following are basic elements and units which can be constructed with the aid of magnetic cores:

a) Register,
b) Dynamic flip-flop,
c) Logical circuits "both-and," "either-or," "negation," etc.,
d) Magnetic memory,
e) Address systems (decoders).

3. Basic characteristics of the elementary circuits are:

a) Input signals,
b) Output signals,
c) Required power,
d) Range of frequencies,
e) Flip-Flops.

4. Technical and economical considerations of computers utilizing magnetic cores as well as the level of the design of circuits reached by now permit the recommendation of the mass production of such units and blocks which would result in broad and immediate application of high-speed computers in the nation's economy, thus improving it.

In order to solve this problem the possibility of commercial-scale production has to be considered.

PGEC Membership Survey*

W. L. MARTIN† AND S. R. OLSON†

A survey of the membership of the PGEC was made during late summer of 1956. The purpose of the survey was to gather a variety of facts about the general membership, so the management of the PGEC could better serve the needs of its membership. Information on membership distribution, area of interest, background and training, and other such factors were needed and were also recognized to be of interest to the membership directly.

Accordingly, an *ad hoc* committee was established in the summer of 1955 to prepare a proposal for a survey to include all factors that would be of interest. After many cycles of discussion between committee members, national officers, and local officers, the form shown in Figs. 1 through 4 (pp. 50–53), was accepted. In August of 1956, 4977 such forms were mailed out to all members of the PGEC according to the national headquarters roster. Business reply envelopes were provided for return of the survey forms to Price Waterhouse and Co., San Francisco, Calif.

On October 15, 1956, the returns were counted, separated, as shown on the form, and mailed to the Rand Corporation for tabulation of the data. A total of 2519 forms was received. Many forms had more than one check where only one had been requested so that some of the information does not tally with the total number of returns. When such multiple checks were encountered, all were counted.

In a survey such as this one, discrepancies of this kind are probably trivial compared to the semantics problem of interpreting the form, experienced by each person filling it out. Accordingly, each of you will probably draw somewhat different conclusions from the results.

It is obvious that many interesting cross-plots can be obtained from the data gathered. Selected families of information are presented in this report. Items 3, 4, 6, 9, and 17 are displayed in the form of histograms. If interest exists, subsequent reports can present further different breakdowns of this information.

Item 1

	Directly	Indirectly	No
Is your job concerned with analog computers?	512	706	1301
Is your job concerned with digital computers?	1402	724	393

Item 2

How are you involved with computers?

Producer	1372
User	558
Consultant	178
Educator	67
No answer	344

Item 3

Phase of computer field
See Fig. 5. (p. 54)

Item 4

Nature of work
See Fig. 6 (p. 54).

Item 5

Employer

Private industry (commercial)	1011
Private industry (military)	944
Educational institute or endowed research organization	305
Government (civilian, local, or federal)	165
Armed service (noncivilian)	61
No reply	33

Item 6

Size of company (total number of employees)
See Fig. 7. (p. 54).

Item 7

Annual basic salary (619 did not reply)

Annual basic salary was defined on the survey form as including normal bonus, if any, but not overtime pay. In Fig. 8 (p. 54), the first family of curves shows the 10th, 50th, and 90th percentile groups of 1900 members reporting. The 90th percentile line, for example, can be considered a boundary between the highest paid 10 per cent of the surveyees and the remaining 90 per cent. In Fig. 9 (p. 54), the second family of curves shows the 50th percentile in annual basic salaries for 1808 reporting members with Doctor's, Master's, and Bachelor's degrees, one curve representing each kind of degree. It should be stated that not enough replies were received from people with extensive experience to provide a good sample, especially for the highest degree.

Item 8

Number of professionals in your company

1–10	389
11–50	413
51–100	218
101–250	234
251–1000	245
Over 1000	248
No reply	772

Item 9

Educational background

Information gathered on this item was modified before plotting to indicate only the highest degree possessed by the members in each classification. (Fig. 10, p. 54.)

* Manuscript received by the PGEC, December 11, 1956.
† Marchant Research, Inc., Oakland 8, Calif.

THE INSTITUTE OF RADIO ENGINEERS
INCORPORATED
1 EAST 79 STREET
NEW YORK 21, N.Y.

9 August 1956

To: Members
Professional Group on Electronic Computers

Subject: Membership Activities Survey

The Professional Group on Electronic Computers of the IRE wishes to make a survey of its members to determine their backgrounds, interests, the nature of the organizations they represent, their professional status and other factors so that it can better serve their needs. This questionnaire will make it possible to tabulate a wide range of such data which will be of significant interest to each member and to those people in the membership planning various meetings and activities concerned with computers.

No information which might serve to identify either individuals or individual companies is desired. The boxed numbers after each item on the survey form are only for the convenience of coding the information when the data is reduced. In order to guarantee the anonymity of the form, all mail will be returned in the business reply envelope provided to Price Waterhouse & Co., a nationally known firm of certified public accountants. Price Waterhouse & Co. will separate the forms as indicated on the tear lines and mail to Rand Corporation, a non-profit research organization which has offered to perform the data analysis as a free service.

Survey information received after October 1, 1956, cannot be included in this tabulation.

Results of the survey will be published in subsequent issues of the TRANSACTIONS of the PGEC.

Thank you for your cooperation.

Very truly yours,

William L. Martin

William L. Martin - Chairman
PGEC SURVEY COMMITTEE

WLM:dc

Fig. 1.

THE INSTITUTE OF RADIO ENGINEERS, INC.

PGEC MEMBERSHIP SURVEY

Please do not indicate your name or company affiliation.

Complete this form by October 1, 1956 and mail it in the envelope provided to:

Price Waterhouse & Co.
120 Montgomery Street
San Francisco, California

Please check (√) appropriate places.

1.

	Directly		Indirectly		No	
Is your job concerned with analog computers		1		2		3
Is your job concerned with digital computers		1		2		3

Please indicate with a check (√) if you are in any of these categories concerned with computers.

2.

Producer		1
User		2

Consultant		3
Educator		4

3.

Phase of Computer Field (General Nature of Computer Equipment)	Phase Most Actively Engaged in Professionally -Please check one-		Phase Most Interest In -Please check one-	
Input Equipment		1		1
Output Equipment		2		2
Central Equipment		3		3
Data Storage		4		4
Data Transmission		5		5
Applications		6		6
Systems		7		7
Varied Activities		8		8
Others (Specify)		9		9
Allied Field (Specify)		10		10

4.

Nature of Work	Nature of Work Most Actively Engaged In -Check no more than 2-		Nature of Work Most Interested In -Please check one-	
Electronic Design		1		1
Mechanical Design		2		2
Logical Design		3		3
Mathematics or Programming		4		4
Field Engineering		5		5
Production and/or Fabrication		6		6
Management - Technical		7		7
Management - Administrative		8		8
Sales		9		9
Teacher		10		10
Other (Specify)		11		11

Fig. 2.

5.

Employer	Please Check One	
Private Industry (Predominantly Commercial Work)		1
Private Industry (Predominantly Military Work)		2
Educational Institute or Endowed Research Organization		3
Government (Civilian - Local or Federal)		4
Armed Services (Non-Civilian)		5

6.

Size of Company (If Industry)					
1 - 100		1	1001 - 2500		4
101 - 500		2	2501 - 10,000		5
501 - 1000		3	Over 10,000		6

7.

Annual Salary	Basic *		Total	
$3000 - $3999		1		1
4000 - 4999		2		2
5000 - 5999		3		3
6000 - 6999		4		4
7000 - 7999		5		5
8000 - 8999		6		6
9000 - 9999		7		7
10000 - 11999		8		8
12000 - 14999		9		9
15000 - 20000		10		10
More than 20000		11		11

* Include normal bonus, if any, but not overtime in reporting "Basic" income.

8.

Estimated Number of (Computer) Professionals in Your Company If Industry					
1 - 10		1	101 - 250		4
11 - 50		2	251 - 1000		5
51 - 100		3	Over 1000		6

9.

Education Background - Indicate Each Degree Received						
Major Field	BS or BA		MS or MA		PhD or DSc	
Engineering		1		1		1
Mathematics		2		2		2
Physics		3		3		3
Other (Specify)		4		4		4

10.

Your Age: ____ years

11.

State years of experience you have had since bachelor's degree or, if no degree, then estimate the equivalent number of years of experience: ________ years

12.

Professional Society Membership		
IRE		1
AIEE		2
ACM		3
SIAM		4
AMA		5
Other (Specify)		6

13.

IRE Professional Group Membership								
PGA		1	PGI		1	PGMTT		1
PGBTS		2	PGTRC		2	PGMedE		2
PGAP		3	PGANE		3	PGCS		3
PGCT		4	PGIT		4	PGUE		4
PGNS		5	PGIE		5	PGCP		5
PGVC		6	PGEM		6	PGPT		6
PGRQC		7	PGED		7	PGAC		7
PGBTR		8	PGEC		8	PGMilE		8

Fig. 3.

14.

Which of the following professional meetings or conferences do you normally attend ?	Please check	
Eastern Joint Computer Conference		1
Western Joint Computer Conference		2
IRE National Convention		3
WESCON		4
ACM National Meeting		5
AIEE National Meeting		6

15.

What geographical area are you employed in ?											
Eastern U.S.		1	Middle U.S.		2	Western U.S.		3	Outside U.S.		4
Including: Maine, N.H., Vt., Mass., R.I., Conn., N.Y., N.J., Pa., Del., Md., D.C., W. Va., N.C., S.C., Ga., Fla., Atlantic U.S. Possessions			Including: N.D., S.D., Nebr., Kan., Okla., Tex., La., Miss., Ala., Ark., Tenn., Mo., Ky., Ohio., Ind., Ill., Iowa, Wisc., Minn., Mich.			Including: Wash., Ore., Cal., Nev., N.M., Utah, Colo., Wyo., Idaho, Mont., Ariz., Pacific U.S. Possessions					

16.

Data for PGEC TRANSACTIONS Editor:	Yes		No	
Do you usually check the contents of each of the TRANSACTIONS on Electronic Computers sufficiently to know the subject matter of the papers ?		1		1
Do you feel that there should be more analog papers in comparison to digital papers ?		2		2
Do you feel that there should be more digital papers in comparison to analog papers ?		3		3
Do you feel that the level of accepted papers is too high ?		4		4
Do you feel that the level of accepted papers is too low ?		5		5
Do you feel that more papers on practical circuits and operating systems characteristics should be encouraged ?		6		6

Note: The information below this line will be separated from the rest of the survey form before any analysis or tabulation is begun.

17.

PGEC Chapter Membership								
Boston		1	Washington		6	Dallas-Ft. Worth		1
New York		2	Akron		7	Houston		2
Philadelphia		3	Detroit		8	Los Angeles		3
Baltimore		4	Chicago		9	San Francisco		4
Montreal		5	Pittsburgh		10	Dayton		5

If your needs for technical meetings are not presently served by a PGEC Chapter, what would be the nearest large city that you feel could support a new Chapter ?

18. ______________________________

City State

Fig. 4.

Fig. 5—Phase of computer field.

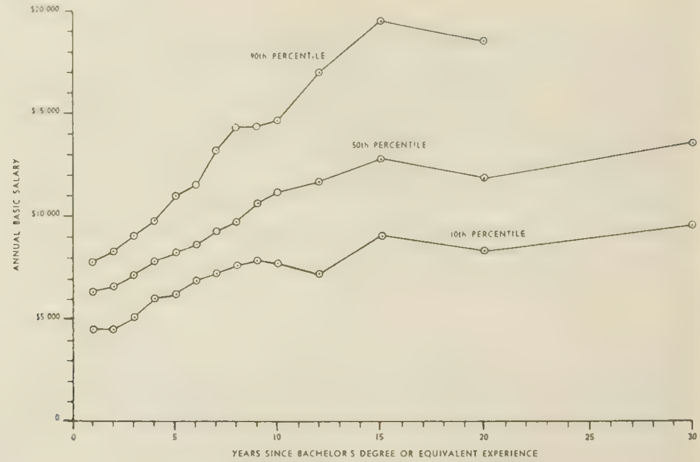

Fig. 8—Annual basic salary, all members.

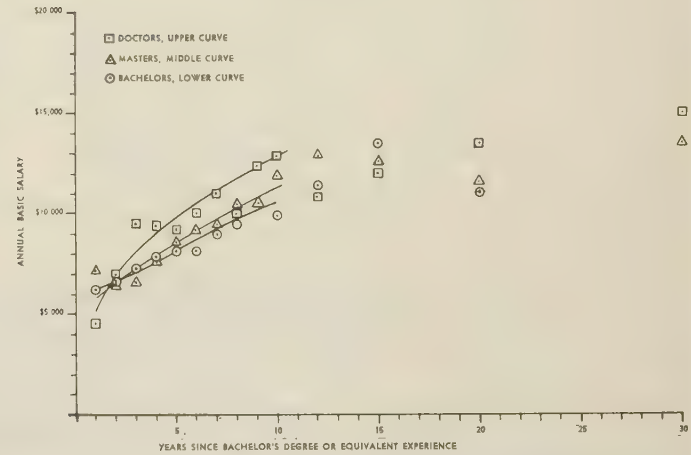

Fig. 9—Annual basic salary; 50th percentiles for members having Doctor's, Master's, or Bachelor's degree.

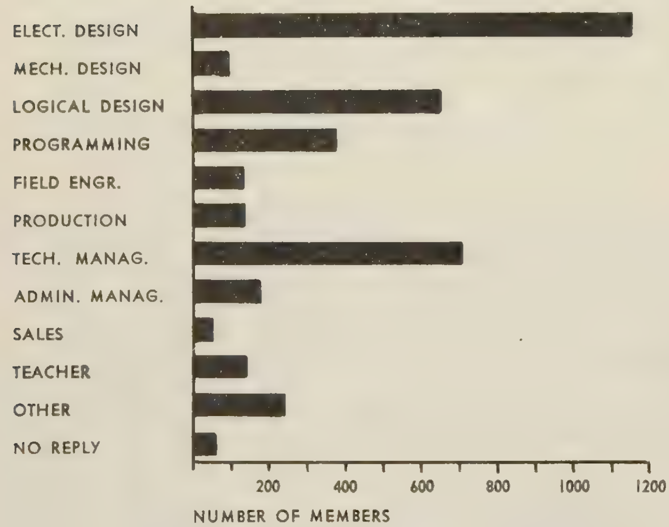

Fig. 6—Nature of work.

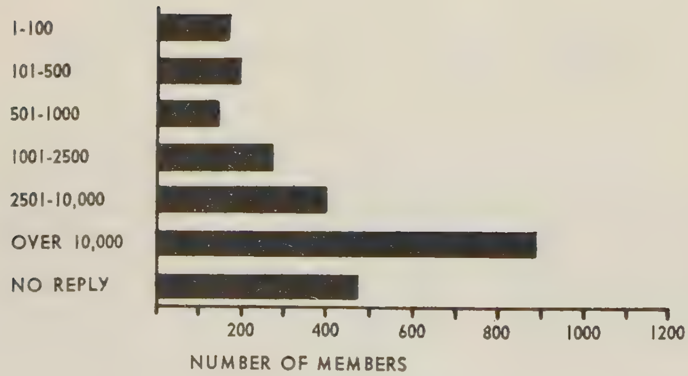

Fig. 7—Size of company.

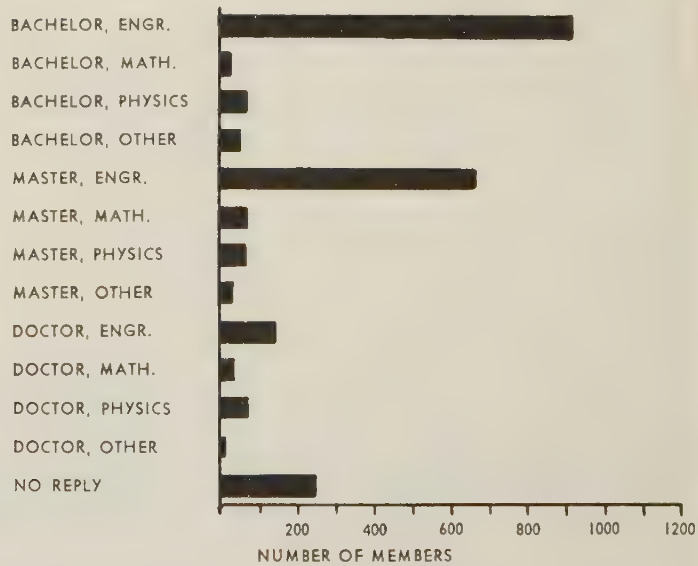

Fig. 10—Educational background.

Item 10—
and
Item 11—

These referred to age and years of experience and were requested so as to correlate with salary and education information.

Item 12—Professional Society membership

IRE	2506
AIEE	588
ACM	384
SIAM	148
AMA	59
Other	362
No reply	11

Item 13—Professional Group membership

PGA	244	PGI	252	PGMTT	80
PGBTS	23	PGTRC	153	PGMED	126
PGAP	66	PGANE	183	PGCS	84
PGCT	526	PGIT	444	PGUE	33
PGNS	93	PGIE	109	PGCP	82
PGVC	32	PGEM	281	PGPT	39
PGRQC	80	PGED	224	PGAC	269
PGBTR	55	PGEC	2385	PGMIL	205

No reply: 51.

Item 14—

Meetings usually attended

The indication of light attendance at western meetings is probably accounted for by the relatively small proportion of forms returned by western members.

EJCC	649
WJCC	276
IRE National	857
Wescon	162
ACM National	7
AIEE National	18
No reply	550

Item 15—

Geographical area employed in

Eastern	1443
Middle	390
Western	597
Foreign	74
No reply	2

Item 16—

This requested information for the PGEC TRANSACTIONS editor. Results indicated general satisfaction except that more papers on practical circuits and operating systems were requested.

Item 17—

Chapter membership
See Fig. 11.

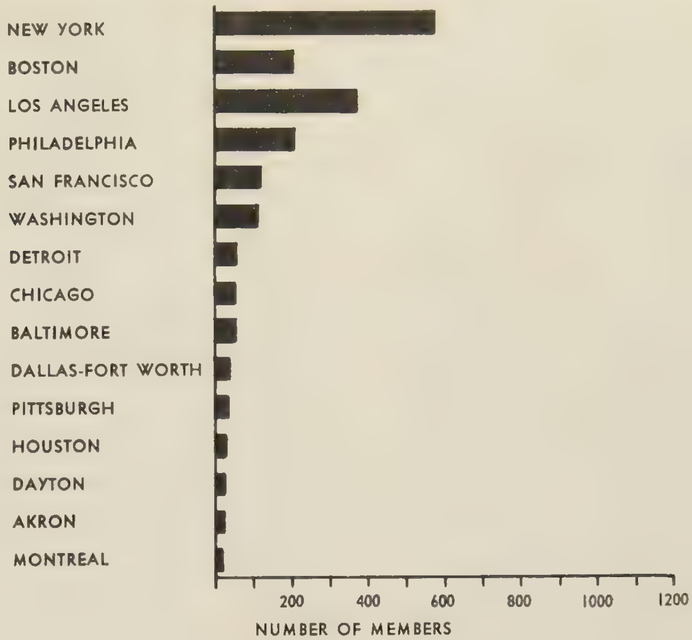

Fig. 11—Chapter membership.

Item 18—

This requested information on areas which might support a new chapter. The following areas having 11 or more requests are listed with the number of requests associated with them.

San Diego, Calif.	14
Atlanta, Ga.	12
Minneapolis—St. Paul, Minn.	19
Poughkeepsie, N. Y.	43
Syracuse, N. Y.	24
Binghamton, N. Y.	13
Buffalo, N. Y.	11
Cleveland, Ohio	12

Scattered single requests were received from the following foreign countries: England, France, Germany, Italy, Japan, and Switzerland.

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The authors wish to acknowledge the assistance of the National Administrative Committees of the PGEC for both 1955 and 1956. The cooperation and efforts of Willis Ware, William Gunning, Jean Felker, and Roger Sisson were especially appreciated in carrying out this survey. The Rand Corporation, Santa Monica, Calif., assisted materially in this project by contributing the necessary machine time and manpower required for tabulation of the survey data.

Review of Electronic Computer Progress During 1956*

INTRODUCTION

Probably the most noticeable development in the digital computer field over the last year or two has been the extension of the art in the direction of larger, more complex, and more ambitious computer systems. The announcement in 1955 of the ultrahigh-speed LARC by Sperry-Rand and the departmentalized BIZMAC by Radio Corporation of America [1, 2] has been followed in 1956 by the International Business Machine announcement of a 10-megacycle multiple-memory transistorized computer STRETCH [3]. These are no longer simply bigger and faster single computing machines; they are in fact versatile computer systems making use of old and new devices in a complex hierarchy of logical and circuit organization. Digital computer development has arrived at the threshold of "corporate structure."

Meanwhile, "mergers" of data-handling equipment have also been taking place. During 1956, Sylvania Electric Products unveiled a processing system with its hub at Camillus, N. Y., and a nationwide 18,000-mile private communication network; the network connects 71 plants and offices in 20 states to a Univac which gathers, records, computes, and classifies a great variety of business activity. The Signal Corps announced successful radio transmission of punch card data between Tobyhanna, Pa., and Orleans, France, with a resultant saving of up to 25 days in administrative handling and transmission time; the radio link will be expanded by wire to include Philadelphia, Pa., Decatur, Ill., Lexington, Ky., and Sacramento, Calif., on a minute to minute logistic basis. The Toronto Stock Exchange automated its operations through a magnetic drum computer which stores current data, updates the storage from keyboard units, and continuously displays the status of every stock both on the Exchange board and in subscribers' offices [7].

In spite of the growing complexity and capability of digital computers, physical size and power dissipation have been maintained and even decreased. This is due mainly to the commercial availability of high-fre-

* Manuscript received by PGEC, January 14, 1957. Prepared by staff members of The Moore School of Elec. Eng. and the Inst. for Cooperative Res., University of Pennsylvania, Philadelphia, Pa.

quency transistors and the development of miniaturized magnetic core switches. The visionary prediction[1] of a complete computer in a filing cabinet drawer has become a soon-to-be-achieved reality, and may already exist as a partly assembled machine in a company laboratory [144].

Diversification in design is another sign of the times. A real effort has been made to optimize different computers for business, scientific, or control applications. More attention is being paid to auxiliary equipment, particularly for business machines [71, 73].

In the analog computer field, the major developments of 1956 may be characterized as speed, streamlining, and semiconductors. Most significant in speeding up analog systems has been the development of automatic equipment setup devices; faster flight tables and digital-analog conversion equipment has also contributed, along with mathematical studies that facilitate the location of errors and equipment malfunctions.

Streamlining has resulted from better methods of miniaturization and packaging that aid trouble-shooting. The availability of neatly packaged, medium accuracy, small-scale analog computers has opened up research and development applications outside the electronics industry. Transistors have found application as amplifiers for current-type analog computers and as switches in electronic multipliers, with better than 1 per cent accuracy achievable.

Although large analog computers have generally been avoided because of problems associated with interconnecting numerous amplifiers, Wright Air Development Center has announced the procurement of a 400-amplifier system from Reeves Instrument Company. The computer will incorporate error prevention and detection equipment aimed at minimizing human-operator errors, checking the setup, and operating the equipment within optimum voltage range [145].

Computer developments in Europe were reported in considerable detail in two companion articles [145, 146]. It appears that France and the United Kingdom are the European leaders in analog computers but Sweden, Germany, Belgium, Italy, Yugoslavia, and Switzerland are active. Numerous digital computers have been built, some in mass-production (by Ferranti and English Electric Company), and are in use throughout Europe; these computers are not more than a year or two behind the most advanced American machines of their types. It is interesting to note that digital computers are in use in Czechoslovakia, the U.S.S.R., and perhaps Poland, and that four men from the U.S.S.R. Academy of Sciences in Moscow attended the International Analogy Computation Meeting in Belgium, September, 1955.

Noted while thumbing through the *Digital Computer Newsletter* were the following two interesting 1956 developments, among many reported in DCN.[2] On August 6, a complete Univac electronic computing system was flown to Frankfurt, Germany, to open a service center at Battelle Institute, Frankfurt. In this country, the U. S. Army established a Mathematics Research Center at the University of Wisconsin to do research and provide a center of knowledge in numerical analysis, probability and statistics, applied mathematics, and all the facets of operations research.

The year 1956 saw increased concern in the training of users and designers of digital computers. Although several books on the subject appeared, a good textbook or group of textbooks is still not available.

The review for 1955 pointed to the hundreds of articles each year which are specifically concerned with computers. The divergence of interests of users and designers call for a substantial review which individual effort and knowledge cannot provide. Even though several individuals participated in the literature search this year, many journals have not even been referenced; to mention only a few, there are the *Journal of the Society for Industrial and Applied Mathematics* (*SIAM*), *Operations Research*, *National Association of Cost Accountants* (*NACA*) *Bulletin*, and *Harvard Business Review*. The writers apologize for all important omissions and for unwarranted emphasis of personally interesting topics, and hope that the review will nevertheless serve a useful purpose.

Systems

As mentioned in the introduction, a number of digital computer systems have recently been completed or announced. Another development has been a smaller magnetic computer [4] using miniature metallic transformers capable of relatively fast switching. Considerable effort has also gone into the development of more specialized business systems, of which [5] is an example. Larger analog systems are also being built, capable of solving problems with considerably more parameters [8].

Programming

In order to alleviate the programming bottleneck in preparing problems for digital computer solution, several companies have been developing compilers which expedite automatic programming. Examples are the IBM Fortran and the Sperry Rand BIOS and A-2 compilers. Another approach adopted was a cooperative effort by West Coast users, called PACT I, to develop a compiler for the IBM Type 701. The status of this effort has been described in a set of six papers [10]. This joint program is being followed by SHARE, the purpose of which is to facilitate communication through standardization of language and nomenclature and to share programmed routines.

It is well known that there is an isomorphic relation between programming and circuit design; most instructions built into a digital computer could be omitted since they can be programmed as subroutines composed of the more primitive instructions. Existing computers generally represent a balance between economics and flexibility. The suggestion was made [11] that the computer designer provide only the primitive instructions but include facilities which allow the programmer to build more powerful instruction words by judicious concatenation of the primitives.

The use of variable-word-length computers, their advantages and disadvantages, were discussed [17, 18].

Components

An interesting and potentially versatile new component, the "transfluxor," was announced during the year [24]. A transfluxor is a magnetic core with more than one hole provided for control wires. One wire is used for setting the core to the "0" or "1" state; the other wire (or wires) are used to sense the state nondestructively and at large reading-signal amplitudes. Since the device can store any amount of flux between the two extreme states, it can be used to radix larger than two or to store analog quantities indefinitely.

Another novel magnetic component, the "cryotron," was also announced [25]. The cryotron takes advantage of the physical property of certain metals to become superconducting at liquid helium temperatures. The critical temperature is a function of the ambient magnetic field. By winding one superconducting wire in a helix onto a second straight wire, the former is able to control the superconducting state of the latter. Power gain is obtained and nondegenerative switching has been achieved. It is interesting to note that the resistance of the superconducting wire is identically zero, so that absolutely no voltage appears across it and no current flows in nonsuperconducting wires in parallel with it.

Improved magnetic materials and high-frequency transistors were also announced [26, 28, 29, 31], as well as negative-resistance semiconductor devices which behave like gas tubes [30, 142]. A silicon transistor for high-speed switching also appeared [58].

Memories

Most laboratories continued to place major emphasis on magnetic memory devices. The most promising development was the use of evaporated magnetic films onto which the drive and sense wires can be printed [32]. Another development was the use of a core with three holes which permitted the use of coincident-current writing and reading without the usually attendant critical drive requirements [33]; the new cores also made possible access times in the fractional microsecond range and much larger sense signals. Reduction in size and assembly costs of conventional core memories were promised by the development of a molded ferrite apertured plate capable of storing 256 bits per plate (about $\frac{3}{4}$ inch square) [34].

Work continued on ferroelectric memory units [39, 143] and electrostatic storage [40].

Analog Circuits

A number of transistorized operational amplifiers were announced [41, 42, 43]. New function generators were described for transcendental functions, product-quotient, and squaring [45, 46, 48, 54, 55, 56] and several multipliers [48, 49, 50, 51].

[1] By J. Presper Eckert in 1947 (if one's memory unit is reliable).

[2] "In recognition of the valuable information reported in a factual and unbiased manner in the 'Digital Computer Newsletter,' the Council of the Association for Computing Machinery wishes to record its appreciation to the Editor of the Newsletter." *J. Assn. Comp. Mach.*, vol. 3, p. 382; October 1956.

Digital Circuits

A great many papers described new transistor and magnetic switching circuits, demonstrating that this area is still ripe for invention [57, 58, 59, 63]. Counters and scaling circuits occupied considerable space in the literature [61, 62, 67, 68] and a new ultrahigh-speed flip flop appeared [65].

Input-Output

Three different solutions to the problem of large-capacity random-access external memory were offered during the year. IBM announced a juke-box RAM with total storage of 40,000,000 bits on fifty rotating disks and $\frac{1}{2}$ second average access time [71]. Potter offered a 500,000,000 bit storage on 200 Mylar-base magnetic tapes, also with $\frac{1}{2}$ second average access time [147]. Burroughs made available a Datafile System storing over 1 billion bits with somewhat slower average access of 5 to 10 seconds [73]. Three digital printers and display devices appeared [74, 75, 76] and many varied analog recorders [81, 82, 83].

Logical Design and Switching Theory

The major emphasis in logical design of digital computers was for higher speeds, both to permit solutions in real-time [84, 85] and to make possible the solution of more complex problems, particularly those involving partial differential equations (LARC and STRETCH). Meanwhile a great deal of attention was paid to logical design theory. An important paper in two parts [89] presented a detailed discussion of principles and practice of using redundant networks of "crummy" switches to obtain reliable system operation [89]. Another paper [94] generalized the work of Hamming by using group theory to generate error-detecting and error-correcting codes.

Applications of Analog Computers

Mixed analog-digital systems appeared more often in the literature [97, 116], and methods for extending the usefulness of analog computers were described [100, 101, 103, 107]. Although it is usual to think of digital computers serving to provide checks on analog setups, an interesting paper [98] describes the use of analog computers to simulate a digital filter. Meanwhile analog computers continued to solve important engineering problems in large numbers.

Applications of Digital Computers

The uses of digital computers continued to grow more diversified. Existing computers were used to simulate the behavior of proposed new digital computers [108]. Language translation was extended to include Chinese, and translations into Russian were reported from Moscow [110–113]. Digital simulation became better understood and more widely used [116, 117, 118], and the simulation of human behavior has received wide attention [120, 121].

The book "Automata Studies" [121] is a collection of research articles by authors with backgrounds in logic, mathematics, physics, engineering, neurology, and psychology, with the theory of automata as the central theme. Papers which deal with automata as synthetic individuals simulated by digital computers include J. von Neumann's "Probabilistic Logics and the Synthesis of Reliable Organisms from Unreliable Components" [*cf.* 89]; M. L. Minsky's "Some Uneconomical Robots," in which a simulated robot is given a limited lifetime T; E. F. Moore's "Gedanken-Experiments on Sequential Machines," in which machines are studied by means of observed input-output stimulus-response relationships, a topic directly related to minimizing switching circuits for digital computers; C. E. Shannon's "A Universal Turing Machine with Two Internal States," which shows that any Turing machine computation can be done by a simple machine with only two states and a large tape alphabet; and "Computability by Probabilistic Machines" by de Leeuw, *et al.*, which shows that computers taking advantage of random-number generators do not become capable of computing anything that an ordinary Turing machine cannot compute, as long as the random number generator is described in terms of a computable probability.

Sampled-Data Control Systems

Mixed analog-digital systems were becoming almost commonplace as control units in automatic production systems. Many articles appeared, some tutorial in nature and some representing mild advances in theory and technique.

Miscellaneous

Reliability in design and production, and faster methods for ascertaining reliability continued to occupy the attention of some authors [131, 132, 133]. The training bottleneck was becoming more severe and increased attention was directed to the problem [134–138, 148], but appreciably more must be done before the situation will improve.

Greater interest was shown in European developments, which appeared to be well worth watching for novel ideas and new devices [145, 146].

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His main interest has been in the field of computers. He spent two years on the IBM, SSEC computer, and for four years worked at the Institute for Advanced Study in Princeton, N. J., where he designed the input-output system and a magnetic drum memory for the IAS computer. The following year he joined the magnetics group at RCA Laboratories at Princeton, where he worked on magnetic logic circuits, and is now a member of the ERMA computer group at Stanford Research Institute in Menlo Park, Calif.

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Stanley P. Frankel (M'55) was born in Los Angeles, Calif., in 1919. He received the B.A. degree in 1938 and the Ph.D. degree in 1942, both in physics from the University of California. From 1942 to 1946 he worked for the Manhattan District, U.S.E.D., at the University of California Radiation Laboratory and at Los Alamos. He was on the staff of the Institute of Nuclear Studies of the University of Chicago from 1946 to 1947 and the Engineering Division of the California Institute of Technology from 1949 to 1954. From 1947 to 1949 he was a member of Frankel & Nelson, consulting in mathematical physics. Since 1954, he has acted as consultant to the Continental Oil Company, primarily in mathematical physics, and to a number of companies in the digital computer field, primarily in logical design.

Since 1943 he has made use of a number of digital computers for the solution of various industrial and scientific problems. From 1949 to 1954 he headed the digital computing group which provided for the digital computing needs of CIT. In the course of this activity he developed the logical design of MINAC which was partially constructed in breadboard. This design was subsequently licenced by CIT to Librascope and forms the basis of their LGP-30, the first production copy of which is now in operation at CIT. During the period from 1954 to the present, he developed the logical design for CONAC, a more powerful magnetic drum digital computer for scientific use. An engineering prototype of CONAC has been built by the Continental Oil Company and is now in service.

He is a member of the American Physical Society, the Association for Computing Machinery, and other professional societies.

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Marcel J. E. Golay (SM'51) was born in Neuchatel, Switzerland, on May 3, 1902. He attended the Gymnase Scientifique of Neuchatel, where he received the B.Sc. degree in 1920, and the Federal Institute of Technology in Zürich, where he received the Lic. El. Engr. degree in 1924.

From 1924 until 1928 he was at the Bell Telephone Laboratories. In 1928 he went to the University of Chicago, where he obtained the Ph.D. degree in physics in 1931.

After a short association with the Automatic Electric Company, Chicago, Ill. Dr. Golay entered the Civil Service, and was a member of the Signal Corps Engineering Laboratores at Fort Monmouth, N. J., until 1955. He is now serving as consultant to the Philco Corporation of Philadelphia, Pa., and to the Perkin-Elmer Corporation of Norwalk, Conn.

Dr. Golay has published numerous articles in the fields of communications, physics, and physical chemistry, and is the holder of numerous patents. He received the Harry Diamond Award of IRE in 1950. He is a member of the American Physical Society, Optical Society of America, American Rocket Society, and Society for Applied Spectrascopy.

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Jan A. Rajchman (SM'46–F'53) was born in London, England, on August 10, 1911. He received his diploma in electrical engineering in 1934 and the degree of Doctor in Technical Sciences in 1938 from the Swiss Institute of Technology, Zurich, Switzerland. He started in the summer of 1935 as a student engineer at RCA Manufacturing Co. in Camden, N. J. In 1936 he joined the staff of RCA Manufacturing Co. as a research engineer and in 1942 he was transferred to the RCA Laboratories in Princeton where he is a member of the research staff. At first he worked in electron optics. He is chiefly responsible for the electron multiplier

tube. During the war he was among the first to apply electronics to computers. Later he worked on the betatron for which he became a co-recipient of the 1947 Levy Medal of the Franklin Institute. After the war he resumed work on computing devices. He developed the selective electrostatic storage tube. Turning to the new field of magnetics he developed the magnetic core memory, magnetic switching circuits, and the transfluxor. He is presently active in the field of magnetics and other solid state devices.

Dr. Rajchman is a member of the American Physical Society, the Council of the Association for Computing Machinery, and Sigma Xi. He holds more than 50 U. S. patents and is the author of many technical papers.

E. LeRoy Younker (M'54) was born on June 14, 1918 in Sidney, Ohio. He received the A.B. degree from Miami University at Oxford, Ohio in 1940 and the A.M. degree in physics from the University of Illinois in 1942.

From 1942 to 1945 Mr. Younker was with the Radiation Laboratory of Massachusetts Institute of Technology.

In November 1945, he joined the Bell Telephone Laboratories where he worked on the development of antennas for fm radio and television transmission. Later he did research in the use of electronic switching techniques in telephone central offices. Since 1953 he has been concerned with the application of transistors to airborne digital computers.

Erich S. Weibel was born July 5, 1925, in Switzerland. In 1948 he received the M.S. degree in theoretical physics from the Swiss Federal Institute of Technology, in Zurich. In 1954, he was awarded the Ph.D. degree in mathematics from the same institute for his work in the theory of elastic shells. Dr. Weibel came to this country in 1951 when he joined the General Electric Company. From 1953 until September, 1956, he served as a member of the technical staff of the Bell Telephone Laboratories, Inc., Murray Hill, N. J. He is now a member of the technical staff of the Aeronautical Research Laboratory, at the Ramo-Wooldridge Corporation in Los Angeles, Calif. Dr. Weibel's work has been in the theory of elastic shells, underwater sound and speech coding.

PGEC News

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Second National Simulation Conference

The Second National Simulation Conference, sponsored by the PGEC, will be held at the Shamrock Hilton Hotel, Houston, Texas, on April 11–13, 1957, concurrently with the Ninth Southwestern IRE Conference and Electronics Show. The deadline for papers has passed, but inquiries about the conference may be directed to Frank C. Smith, Jr., P.O. Box 13058, Houston 19, Texas.

Association for Computing Machinery Twelfth Annual Meeting

The Association for Computing Machinery has accepted an invitation from the University of Houston to hold its Twelfth Annual Meeting on the campus at Houston, Texas, on June 19–21, 1957. Local arrangements will be under the direction of James G. Steward, Standard Oil Company of Texas, Houston 1, Texas. The deadline for papers has passed.

International Association for Analog Computation

Word has been received of the formation in Brussels, Belgium, of the Association Internationale Pour le Calcul Analogique. Interested persons should communicate with the Secretary General, F. H. Raymond, Societe d'Electronique et d'Automatisme, 138 Boulevard de Verdun, Courbevoie (Seine), France.

PGEC Sponsored Fellowship

During the past two years, negotiations have been completed which enable the PGEC to sponsor an annual Fellowship for graduate study in computing. The amount of the stipend will be $2000 plus tuition not to exceed $1000. Initially this Fellowship is to be underwritten by the PGEC for two years, although it is hoped that it can be supported on a continuing basis.

This Fellowship will be administered through the Office of Scientific Personnel of the National Academy of Sciences, and the selection of the successful recipient will be made by that office. It is expected that the first Fellowship will be awarded for the 1957–1958 academic year. There will be no restrictions as to the university or college to be attended, but it will be necessary for the Fellow to specialize in computing or a closely allied field.

Applications for this Fellowship should be addressed to:

Fellowship Office
Office of Scientific Personnel
National Academy of Sciences
2101 Constitution Avenue, N.W.
Washington 25, D. C.

Announcements made by the National Academy of Sciences will not mention this Fellowship by name but will merely indicate that the National Academy Fellowship program has available a number of fellowships, of which this is one. The PGEC is publicizing this Fellowship directly through its own Transactions, the IRE Student Quarterly, Proceedings of the IRE, and through each PGEC Chapter.

Willis H. Ware, *Chairman*
Student Activities, PGEC

Symposium on Information Retrieval Systems

A Symposium on Systems for Information Retrieval will be held on April 15–17, 1957, by Western Reserve University in cooperation with the Council on Documentation Research and numerous other organizations. In addition to the program of papers, there will be exhibits of working equipment. The symposium will be held at Masonic Auditorium, 3615 Euclid Ave., Cleveland, Ohio. For further information, contact Jesse H. Shera, School of Library Science, Western Reserve University, 11161 East Boulevard, Cleveland 6, Ohio.

Reviews of Current Literature

It is the intention of this section to review articles that have been published since January 1, 1953, and to publish eventually reviews of all books pertaining to the computer field. Authors can be of considerable assistance in this review process by sending two reprints of their articles to H. D. Huskey, Department of Electrical Engineering, University of California, Berkeley, California. The editors wish to express their gratitude to the reviewers who, through their efforts, make this section possible.—*H. D. Huskey*

GENERAL

57-1

IRE Standards on Electronic Computers: Definitions of Terms, 1956—(Proc. IRE, vol. 44, pp. 1166–1173; September, 1956.) This is the list of official definitions of approximately 175 digital computer terms.

A. D. Scarbrough

57-2

Tube-Characteristic Changes and Equipment Reliability—The Applications Engineers of the Advisory Group on Electron Tubes. (*Tele-Tech* and *Electronic Ind.*, vol. 15, pp. 96–97, 346–348; June, 1956.) A brief article warns that the ideal and only sure way to predict reliability is to "test all electron tubes to destruction under conditions identical to those encountered in the actual equipment." This method has the disadvantage that there are no tubes left to use in the equipment. That's one way to solve the problem. Statistical data of any kind on changes in tube characteristics with life are very scarce. This article presents data on tubes run at full-rated dissipation at 165°C. bulb temperature. The results are presented in the form of cumulative frequency distribution (ogive) curves. A family of these curves gives per cent survival for various definitions of death vs the number of hours tested. The tube types included are the 5654/6AK5, 5718, 5719, 5751, 5840, 6101/6J6WA, and the 6186/6AG5WA. For example, under the test conditions specified, the failure rate for 6AK5 tubes is 18 per cent per 1000 hours, if death occurs at a 20 per cent reduction in G_m. If the circuit will tolerate a 40 per cent reduction in G_m, the failure rate drops to $\frac{1}{2}$ per cent per 1000 hours. Both of these figures are for the first 1000 hours. Most computer applications use tubes under considerably less severe conditions. It will, therefore, be difficult to use the results of this investigation directly in predicting computer application life.

W. F. Gunning

57-3

Analogue vs. Digital Techniques for Engineering Design Problems—D. B. Breedon. (*Electrical Eng.*, vol. 75, pp. 814–816; September, 1956.) The purpose of this article is to describe briefly some computer capabilities to engineers. Some of the major characteristics of four types of computers are stated from the user's point of view. The four types of general-purpose computers discussed here are the electric analog computer composed mostly of passive elements, the electronic differential analyzer using operational amplifiers, the externally-stored program digital machine, and the internally-stored program digital machine. The type of computer appropriate for each of several kinds of problems is indicated by a discussion of a few example problems.

Harry Larson

ANALOG COMPONENT RESEARCH

57-4

Analog Computer Amplifier Circuits—Hiroshi Amemiya. (Proc. IRE, vol. 44, p. 1473; October, 1956.) This letter makes the point that the reciprocity theorem permits the interchange of input and output terminals of either input or feedback impedance of an operational amplifier if the gain is sufficient. The author points out that interchanging input and output terminals of the input impedance of the usual constant coefficient multiplier results in much higher input impedance.

A. D. Scarbrough

57-5

Precise Electronic Switching with Feedback Amplifiers—Charles M. Edwards. (Proc. IRE, vol. 44, pp. 1613–1620; November, 1956.) This well-written and informative article gives circuit details and applications for a number of precision switches (one-to-many and many-to-one). All of these circuits utilize feedback amplifiers with the switching element in the forward gain portion of the loop to minimize the effects of the nonlinear characteristics. The success of the technique can be judged from some of the typical performance figures for a modulator, *e.g.*, 0.1 per cent linearity of full scale; 0.1 per cent stability for ±5 per cent plate supply fluctuation.

A. D. Scarbrough

57-6

An Adaptive Servo System—A. H. Benner and R. Drenick. (1955 IRE Convention Record, Part 4, pp. 8–14.) The adaptive servosystem discussed in this article changes its operating parameters from one linear mode to another linear mode depending on whether the input signal corresponds to a steady rate or varying rate process. The servo was designed to sample the output of process control instruments on a time multiplexed basis and also to provide a prediction function during the intervals between readings for the quantities being sampled. Mathematical expressions and graphs are presented, showing that the one set of parameters which is optimum for a given input condition is not optimum for the other input condition. The rms error criterion is utilized to establish the optimum parameters for the two respective input conditions, including the effect of noise in the system. In considering the possibility of using an adaptive servo system in such an application, two principal conditions must be met: 1) "It should be known that the process will be of the constant-speed type a large proportion of its time," and 2) "it should be known that when the process accelerates it will continue to do so for a period of time which is long compared to the time constants of the system." The method of detection to change from one mode to the other is discussed in terms of the probability that the system will produce the minimum transient error consistent with the minimum error due to a wrong decision. Results obtained from the adaptive servosystem show improvements as high as 2.5 to 1 compared with a linear servosystem.

C. M. Edwards

ANALOG EQUIPMENT

57-7

Radioactive Fallout Computer—(*Nat. Bur. Standards Tech. News Bull.*, vol. 40, pp. 56–58; April, 1956.) The geographic distribution of radioactivity due to particles falling from an atomic bomb cloud is mapped on a cathode-ray tube. Input data are the size and shape of the cloud, radioactive distribution in the cloud, and the wind speeds and directions at 20 altitudes. The computer uses high-speed electronic analog techniques.

R. D. Elbourn

57-8

Electrical Analog Computing Machine for Solving Linear Equations and Related Problems—Samarendra Kumar Mitra. (*Rev. Sci. Instr.*, vol. 26, pp. 453–457; 1955.) For the equation $AX=G$ where A is a matrix, G a given vector, a device is set up to obtain the vector X using the Neumann series $1+\Sigma(1-hA)^{\alpha}$, which converges to $h^{-1}A^{-1}$ for a suitable range of the parameter h. From a given $X^{(m)}$, the machine produces $X^{(m+1)}=hG+(1-hA)X^{(m)}$. This is applied in the case A is positive definite. The device pro-

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—*The Editor*

duces the effect of applying a matrix B to a vector X as the voltage output of an ac network. The elements of $X^{(m)}$ appear as potentiometer settings and by a switching arrangement between two banks of elements are used as inputs for the computation of $X^{m-1)}$. The parameter h is chosen on a compromise basis between convergence and accuracy requirements by a rule of thumb. Certain information relative to characteristic values is also available from the operation of the device.

F. J. Murray
Courtesy of *Mathematical Reviews*

UTILIZATION OF ANALOG EQUIPMENT

57-9

A Method of Solving Linear Algebraic Equations on a Vacuum-Tube Integrator—L. I. Gutenmaher, G. K. Kumžinok, and L. S. Klabukova. (*Vyčisl. Mat. Vyčisl. Tehn.*, vol. 2, pp. 230–246; 1955.) (In Russian.) (The reviewer is using his own notation.) Let the rectangular real matrix A of rank m have n rows and m columns $(m \leqq n)$. The author wants to find x minimizing $|A_x - c|^2$, using a vacuum-tube integrator. It is observed that all eigenvalues of the partitioned matrix

$$\mathfrak{A} = \begin{bmatrix} 0 & -A^T \\ A & I \end{bmatrix} \quad (T \text{ denotes transpose})$$

have positive real part, thus insuring stability of the following machine method: Solve the system

$$b\,\frac{d}{dt}\begin{bmatrix} x(t) \\ y(t) \end{bmatrix} + \mathfrak{A}\begin{bmatrix} x(t) \\ y(t) \end{bmatrix} = \begin{bmatrix} 0 \\ c \end{bmatrix}$$

on the integrator. Then $\lim_{\in\to\infty} x(t)$ will minimize $|Ax-c|^2$. If $m=n$ one is solving $Ac=c$ stably without the Gaussian pretransformation to $A^TAx = A^Tc$. Examples of orders 2 to 6 are discussed, with photographs of the oscilloscope.

George E. Forsythe
Courtesy of *Mathematical Reviews*

DIGITAL COMPONENT RESEARCH

57-10

Trends in Computer Input/Output Devices—J. M. Carroll. (*Electronics*, vol. 29, pp. 142–149; September, 1956.) The need for computers to accept data directly from source documents is commonly recognized. The need for output devices capable of producing printed data supplied at modern computer speeds is also evident. The author has gathered material regarding existing high-speed input-output equipment and recent developments which show promise. It is desirable to obtain input for certain data processing systems directly from a source document. Several companies are listed as developing character readers. Character recognition of most existing equipment relies upon uniform size and form of characters; however, it is felt that further development may reduce these restrictions. Other methods of supplying input data from standard forms make use of coded spots, placed on documents, which can be read magnetically, optically, etc. It was apparent from the article that development in the field of high-speed output equipment has yielded a great variety of ideas for producing printed characters. One of the reasons for the variety of ideas seems to be the variety of forms on which output printing is desired. Some techniques used for printing a few characters per line would not be practical when extended to printing say 100 characters per line. The product desired from modern high-speed output equipment is legible data in a form suitable for direct use in business or industry and which needs no further processing after removal from the equipment.

Norman F. Loretz

57-11

High-Density Tape Recording for Digital Computers—(*Nat. Bur. Standards Tech. News Bull.*, vol. 39, pp. 121–124; September, 1955.) 500–600 binary digits per inch are recorded by an NRZ technique using 2-microsecond recording pulses.

R. D. Elbourn

57-12

A Rotating Reading Head for Magnetic Tape and Wire—(*Nat. Bur. Standards Tech. News Bull.*, vol. 39, pp. 116–117; August, 1955; also *Computers and Automation*, vol. 4, pp. 24–27; August, 1955.) A magnetic reading head is mounted in a rotating drum to permit repeated scanning of sections of magnetic tape or wire. Silver sliprings provide low-noise contacts and a photoelectric system provides a jitter-free trigger for an oscilloscope.

R. D. Elbourn

57-13

The Cold-Cathode Gas Diode—(*Nat. Bur. Standards Tech. News Bull.*, vol. 39, pp. 61–66; May, 1955.) NE-2 or NE-51 gas diodes can be used as indicators, oscillators, flip-flops, and-gates, or-gates, or memory elements. Their firing voltages can be equalized by aging in parallel.

R. D. Elbourn

57-14

Diode Amplifier—(*Nat. Bur. Standards Tech. News Bull.*, vol. 38, pp. 145–148; October, 1954.) Several flip-flop circuits are described that are based upon amplification achieved by injecting and subsequently collecting minority carriers in a semiconductor diode.

R. D. Elbourn

57-15

A Survey of the Properties and Applications of Ferrites Below Microwave Frequencies—C. Dale Owens. (Proc. IRE, vol. 44, pp. 1234–1248; October, 1956.) This interesting introductory article to the "Ferrites" issue is reviewed here because it includes survey material on coincident current memories, multiaperature ferrite core devices, and pulse transformers. An extensive bibliography is included which should be helpful to computer engineers using ferrites.

A. D. Scarbrough

537.226/.227:546.431.824-31 57-16

A Microstructure Study of Barium Titanate Ceramics—F. Kulcsar. (*J. Amer. Ceram. Soc.*, vol. 39, pp. 13–17; January 1, 1956.) Polishing and etching techniques for preparing polycrystalline $BaTiO_3$ for metallographic examination are described. Photomicrographs are reproduced and discussed. A companion paper by Cook (*ibid.*, pp. 17–19) analyzes some of the domain patterns found.

Courtesy of Proc. IRE
and *Wireless Engineer*

57-17

P-N-P-N Transistor Switches—J. L. Moll, M. Tanenbaum, J. M. Goldey, and N. Holonyak. (Proc. IRE, vol. 44, pp. 1174–1182; September, 1956.) This article describes the design, fabrication, and electrical characteristics of a silicon *p-n-p-n* structure suitable for use as a two-terminal negative impedance device. Although these devices are not commercially available, computer circuit designers may be interested in a preview of devices potentially useful for flip-flops, oscillators, pulse generators, and the like. Most of the electrical circuit information is in the form of static V-I characteristic curves at various temperatures, but some idea of the frequency response of present experimental units can be obtained from the statement that sawtooth oscillators have been constructed which operated at a repetition rate of 2 mc.

A. D. Scarbrough

57-18

Quarterly Report No. 10, Second Series—J. R. Bowman, W. J. Kirkpatrick, *et al.* (*Quart. Rep. Computer Components Fellowship Mellon Inst.*, 47 pp.+ix; January 1, 1956 to March 31, 1956.) Part I contains six sections related to the preparation and testing of graphic circuits for high temperature use. Vacuum evaporation and deposition of conducting and dielectric materials, and the silk screen printing of ceramic enamels have been used to prepare modular units consisting of resistors, capacitors, and conducting leads; while stannic oxide resistors have been prepared by spraying acetone solutions of tin chloride onto a heated substrate. Part II continues the work on electroluminescent films. The results of measurements of the effect of various metal electrode backings on electroluminescent cells are presented. Screens made from uranyl nitrate were tested in fields as high as 170,000 volts per cm at 60 cycles per second, but no electroluminescent light was detected.

C. H. T. Wilkins

57-19

Quarterly Report No. 11, Second Series—J. R. Bowman, W. J. Kirkpatrick, *et al.* (*Quart. Rep. Computer Components Fellowship Mellon Inst.*, 73 pp.+viii; April 1, 1956 to June 31, 1956.) The report is divided into two major parts. The first deals with graphic circuitry for high temperature use, while the second continues work on electroluminescent phenomena. Part I: Aluminum and silver conductor films were found to have a tendency, respectively, to oxidize and to migrate at temperatures above 200°C.; gold conductors, prepared both by the silk screen process and by vacuum evaporation-deposition, were stable and performed satisfactorily. Capacitors with lead borate glass and ti-

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—*The Editor*

tanium dioxide-lead borate glass dielectrics were prepared by the screen process. An apparatus for the flash-evaporation of alloy resistors in vacuo is described. Boron carbide resistors by the screen process were reproducible and stable up to 260°C. Resistors were prepared by removal of undesired portions of a uniform stannic oxide surface film. A convenient method of composing various resistor materials, based on an empirical equation in the literature, is outlined. A list of papers and patents on stannic oxide films is included. Part II: The brightness wave characteristics of an electroluminescent cell vary with the different metals used as a back electrode. These characteristics do not follow any apparent trend with the work function of the metal electrode, whereas high "phosphor" brightness is generally favored by metal backing of high work function.

C. H. T. Wilkins

DIGITAL SYSTEM RESEARCH

57-20

Reflected Number Systems—Ivan Flores. (IRE Trans., vol. EC-5, pp. 79–82; June, 1956.) Many papers have been written about the reflected binary system and it is well known in the computer field for analog-to-digital conversion. The method used in creating this system may be extended to systems of bases other than two. It is the purpose of this paper to carry this extension to its logical conclusion. The author describes how reflected systems of different bases may be composed. The equations for translating between the conventional and reflected systems are then derived. It is also demonstrated how the reflected binary system is a special case of reflected number systems and how the general case simplifies for the reflected binary case.

Courtesy of Proc. IRE

57-21

Mathematical Foundations and Computational Methods for a Digital Logic Machine—Robert S. Ledley. (*J. Operations Res. Soc. of Amer.*, vol. 2, pp. 249–274; August, 1954.) Although methods for formulating and analyzing logical problems algebraically are well known, practical difficulties often prevent complete solutions when the number of variables involved is at all large. After reviewing the fundamentals of the two-valued propositional calculus, this paper outlines numerical procedures for systematically dealing with such problems. The procedures described are based on associating with each variable a "designation number" consisting of a series of 1's and 0's. Rules are given for developing the corresponding designation numbers for any logical combination of the basic variables. Logical problems can thereby be analyzed numerically by appropriate manipulation of the designation numbers. Specific applications discussed include simplification of algebraic expressions in terms of products of sums or sums of products, change of variables, solution of simultaneous equations, and generation of the "absolute simplest form" (minimum number of $+$ and $\cdot$ operations). Several examples of complex logical problems are given to illustrate the use of these techniques. At the close of the paper, the author discusses means for handling the manipulation of designation numbers by hand computation, by desk calculators, and by automatic computers. The principle of designation numbers is suggested as the basis for a new type of computer for logical problems.

E. C. Johnson

681.142 57-22

The Logical Design of an Idealized General-Purpose Computer, Part I—Arthur W. Burks and Irving M. Copi. (*J. Franklin Inst.*, vol. 261, pp. 299–314; March, 1956.) This part of the paper describes a computer with a very primitive order code which permits simple arithmetic and shift operations to be performed on 16-bit numbers in the arithmetic unit, and to address 4095 words in static storage and one word in sequential storage, which occupies the 4096th address position. The instruction code permits moving the sequential storage backward and forward. The logical elements employed are luxurious, and the aim of the paper appears to be to describe all elements of the computer in terms of logical descriptives to provide a rigorous description of all phases.

Gene M. Amdahl

681.142 57-23

The Logical Design of an Idealized General-Purpose Computer, Part II—Arthur W. Burks and Irving M. Copi. (*J. Franklin Inst.*, vol. 261, pp. 421–436; April, 1956.) This part of the paper starts with the declaration that the machine's arithmetical operations of add, subtract, halve, and double are adequate to perform more complex operations such as multiply and divide. Some demonstration of this is shown. The discussion then goes to the logical description of the arithmetic operations and of the address counter and control. No unified logical description of the computer executing a routine is given. The conclusion of the article is that a rigorous diagrammatic symbolism was developed which enjoys economy as well as precision and intuitive clarity.

Gene M. Amdahl

DIGITAL EQUIPMENT

57-24

The High-Speed Electronic Calculating Machine of the Academy of Sciences of the U.S.S.R.—S. A. Lebedev. (*J. Assoc. Comp. Mach.*, vol. 3, pp. 129–133; July, 1956.) The description of this machine was first given by Professor Lebedev at the meeting on electronic computers at Darmstadt, Germany, October 25–27, 1955. The design therefore presumably represents the state of the computer art in the U.S.S.R. as of approximately the end of the previous year, 1954. The machine is a three-address binary computer, with floating point logic, an electrostatic memory of 1023 (*sic*) words, and a parallel arithmetic unit of two receiving registers and an accumulator. The word length is 39 bits; 32 for the mantissa, 5 for the characteristic, and two signs. Auxiliary drum and tape units round out the equipment. Enough detail is given to enable the reader to draw a fair mental picture of the machine, but translation difficulties have left several obscure passages in the text. This reviewer was struck by the low speed of revolution of the drum (750 rpm) as well as the relatively low density of information (3 bits per millimeter). The magnetic tape, by contrast, stores at a density of 8 bits per millimeter, and moves 2 meters per second. An "assigning device" of germanium diodes, with a capacity of 276 words, is incompletely described, but its function apparently is to hold needed fixed parameters and other constants for various subroutines. Its contents are initially assigned by punched cards, but are not alterable by the program. The description implies that whole subroutines may be stored in this auxiliary memory. Strangely enough, although the punched cards are used for the germanium memory, punched paper tape provides the primary input to the electrostatic memory. The tape is read photoelectrically at the rate of 20 words per second. A photoprinting device forms an off-line translator for magnetic tape. Results are projected as figures (decimal or alphabetic?) on cinema film, and paper reproductions may be made from this. Characteristic speeds are: 77 microseconds to 182 microseconds for addition and subtraction (including the variable normalization time), 270 microseconds for multiplication, and 288 microseconds for division. Actual addition time is 3 microseconds, and a one-bit shift takes 2 microseconds. These speeds are highly comparable to SWAC, but exceeded by other machines in this country.

F. H. Hollander

57-25

An Automatic Microimage File—(*Nat. Bur. Standards Tech. News Bull.*, vol. 40, pp. 89–90; July, 1956.) A four-digit decimal number from a perforated tape reader causes one of 10,000 frames on a 10-inch-square sheet of microfilm to be enlarged into a $\frac{1}{2}$-inch square and copied photographically onto a 10-inch-wide strip of photosensitive paper. The rate is one frame every two seconds.

R. D. Elbourn

UTILIZATION OF DIGITAL EQUIPMENT

57-26

The Technical Feasibility of Translating Languages by Machine—V. H. Yngve. (*Electrical Eng.*, vol. 75, pp. 994–999; November, 1956.) This article discusses the use of digital computers for language translation. Word-for-word translation is discussed, giving estimates of vocabulary size, and machine requirements. The difficulties encountered in this type of translation are discussed, and it is concluded that the output might be useful but of poor quality. Sentence-for-sentence translation is then discussed, giving an idea of the difficulties encountered here and giving an introduction to the problems of defining language structure. Desirable characteristics for special purpose machines for language translation are mentioned throughout the paper.

Harry Larson

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BOOK REVIEWS

57-27

Digital Differential Analyzers. Part I. Elements. 2nd ed.—George F. Forbes. (Pacoima, Calif., v+54 pp.; 1955.) The booklet is intended to be an application manual for digital differential analyzers. These are electronic machines with a drum memory and with counter-pairs as integrators. Variables are represented by sequences of pulses. The integral $z=\int y dx$ is performed by adding the integrand y to an accumulator whenever a pulse for the variable x appears. The overflows of the accumulator generate the pulses of the z sequence. After explaining the nature of such a machine in more detail the author develops an introduction to the fundamental methods of operating the differential analyzer. This includes scale-factors, the elementary operations of addition, subtraction, multiplication, division, and the generation of functions by means of simple set-ups. Special emphasis is on trigonometric and algebraic functions; Amble's method of inverting functions by regenerative set-ups is also dealt with. The booklet is equipped with many diagrams and with an appreciable number of exercises.

H. Bückner
Courtesy of *Mathematical Reviews*

57-28

Engineering Cybernetics—H. S. Tsien. (McGraw-Hill Book Co., Inc., New York, N. Y., xii+289 pp.; 1954.) This valuable book, written for (actual or potential) research engineers and applied mathematicians, deals with the science of control and communication, which N. Wiener has christened cybernetics. The author deliberately gives a purely theoretical treatment of highly practical topics, as is usually done in fluid mechanics. For example, he recognizes but is not afraid of the fact that some engineers will think the book highbrow, while mathematicians will be disappointed if they expect the rigor and elegance that are customary in abstract mathematics (and in some that is called applied). The principal mathematical prerequisites are of course ordinary differential equations and complex integration; variational methods are also used on occasion. The author has not extended the scope of his work by means of bibliographic material or collections of exercises, but the text itself covers an unusually wide range of topics. This may be indicated by chapter as follows: 1. Introduction. 2. Laplace transform. 3. Transfer function. 4. Feedback servomechanism. 5. Noninteracting controls. 6. Alternating-current and oscillating-control servos. 7. Sampling servos. 8. Time lag. 9. Stationary random inputs. 10. Relay servos. 11. Nonlinear systems. 12. Linear system with variable coefficients. 13. Perturbation theory. 14. Control design with specified criteria (*e.g.*, minimize the time-average of the error-squared). 15. Controls that automatically seek to maximize a criterion of good performance. 16. Filtering of noise (sketches of the Wiener-Kolmogoroff and other theories). 17. Ultrastability and multistability (W. R. Ashby's conception of a system capable of learning in the sense of responding to environmental changes by searching out a stable pattern of behavior for itself). 18. Error control (J. von Neumann's theory of improving the reliability of a system by duplicating or multiplexing its elements). This last study has been extended (to nets of relays) by C. E. Shannon and E. F. Moore in some as yet unpublished work. In Chapter 9 it appears that the author should have had the advice of someone familiar with statistics and probability. The distribution (9.49), often called exponential, is never called Poisson's distribution. Above (9.7), the terms variance and mean deviation should not be used for the standard deviation σ. The most serious lapse noted concerns the concept of ergodicity or metrical transitivity; it not only goes unnamed, but is described as if it were identical with stationarity, or were a consequence thereof. In general, however, the book appears to be adequately clear and accurate. Also, the author has done his duty by a new and growing subject, by including much material (from recent research papers) which has not previously appeared in book form.

E. L. Kaplan
Courtesy of *The American Mathematical Monthly*

57-29

Automatic Digital Calculators. 2nd rev. ed.—A. D. Booth and K. H. V. Booth. (Academic Press, Inc., New York, N. Y., 234 pp.+21 pp. bibliography+5 index pp.+ix; 1956. Illustrated.) (For review of 1st ed., see 54-174, September, 1954 issue.) This book, now in its second revised edition, surveys a large slice of the digital computer field. It includes sections on history, organization, control, arithmetic, input-output, components, circuits, programming, and applications. The subject matter is technical, but the simple style suggests that the book was aimed at the novice. The serious student is aided by an extensive bibliography. To provide detailed illustrations, the authors have understandably borrowed from their experience with the series of computers developed at the University of London, England, which go by such unpronounceable names as APE(X)C. To this are added many examples of different techniques used in other computers. Except for tidbits from the smorgasbord of games, machine learning, and language translation, the programming section is restricted to mathematical applications. There is no attempt to discuss business applications. Since the 1953 edition of the book was written, the computer field has grown tremendously. In the second edition the authors have attempted to keep abreast by inserting new paragraphs on magnetic core and ferroelectric storage, transistors, and automatic programming. Unfortunately they have not succeeded. The book still retains the flavor of the days when there were but a few computers scattered around various universities. It takes no account of the enormous effects of commercial production, both in England and in the United States. The authors' estimates of "current practice" and performance levels have not been revised, and the grafting on of a paragraph on the high-speed NORC computer merely serves to point up the contrast. One can only conclude that writing an up-to-date textbook on digital computers is a herculean task.

Werner Buchholz
Courtesy of Proc. IRE

57-30

Methods in Numerical Analysis—Kaj L. Nielsen. (The Macmillan Co., New York, N. Y., xiii+382 pp.; 1956.) It has become increasingly evident that numerical analysis may now be regarded as having a *raison d'être* in the modern mathematics curriculum. Dr. Nielsen has sought to write *Methods in Numerical Analysis* as an elementary textbook and has approached his objective in a careful and effective manner. As the title implies, the subject matter stresses methodology in the art of computation rather than mathematical sophistication. Appropriate emphasis is placed on those modern computational procedures arising in the analysis of tabulated data and approximate solutions of equations which lend themselves to the use of tables included in the appendix, or are easily adapted to automatic desk calculators for problem laboratory purposes. The first five chapters are concerned primarily with classical material from the theory of errors, accuracy of approximate calculations, finite differences, interpolation theory, numerical differentiation, and integration. Chapters six and seven deal principally with existent procedures for numerical solutions of sets of linear and nonlinear algebraic equations, and an introduction to techniques for handling differential, difference, and partial differential equations. Chapters eight and nine portray some recent developments in the representation of empirical functions and smoothing of data employing the methods of least squares, Nielsen-Goldstein, orthogonal polynomials, and autocorrelation functions. The author apparently believes firmly in systematic procedures and utilizes a multitude of calculating forms and schematics in the topical illustrations which are worked out in detail. In summary, it is the reviewer's opinion that the author has succeeded in writing an effective elementary text and convenient reference on up-to-date methods in the field of numerical analysis, useful for a wide variety of situations encountered by students and workers in applied mathematics.

W. E. Restemeyer
Courtesy of *The American Mathematical Monthly*